

System-on-Chip Design

Data Flow hardware Implementation

Hao Zheng

Dept. Comp Sci & Eng

U of South Florida

haozheng@usf.edu

(813) 9744757

Single-Rate SDF to Hardware

- Single-rate SDF: all production/consumption rates are a fixed number = 1.
 - The entire circuit controlled by a single clock.
- Implementation
 - Actors -> combination circuits
 - Queues -> wires
 - Initial tokens -> registers.

Single-Rate SDF to Hardware

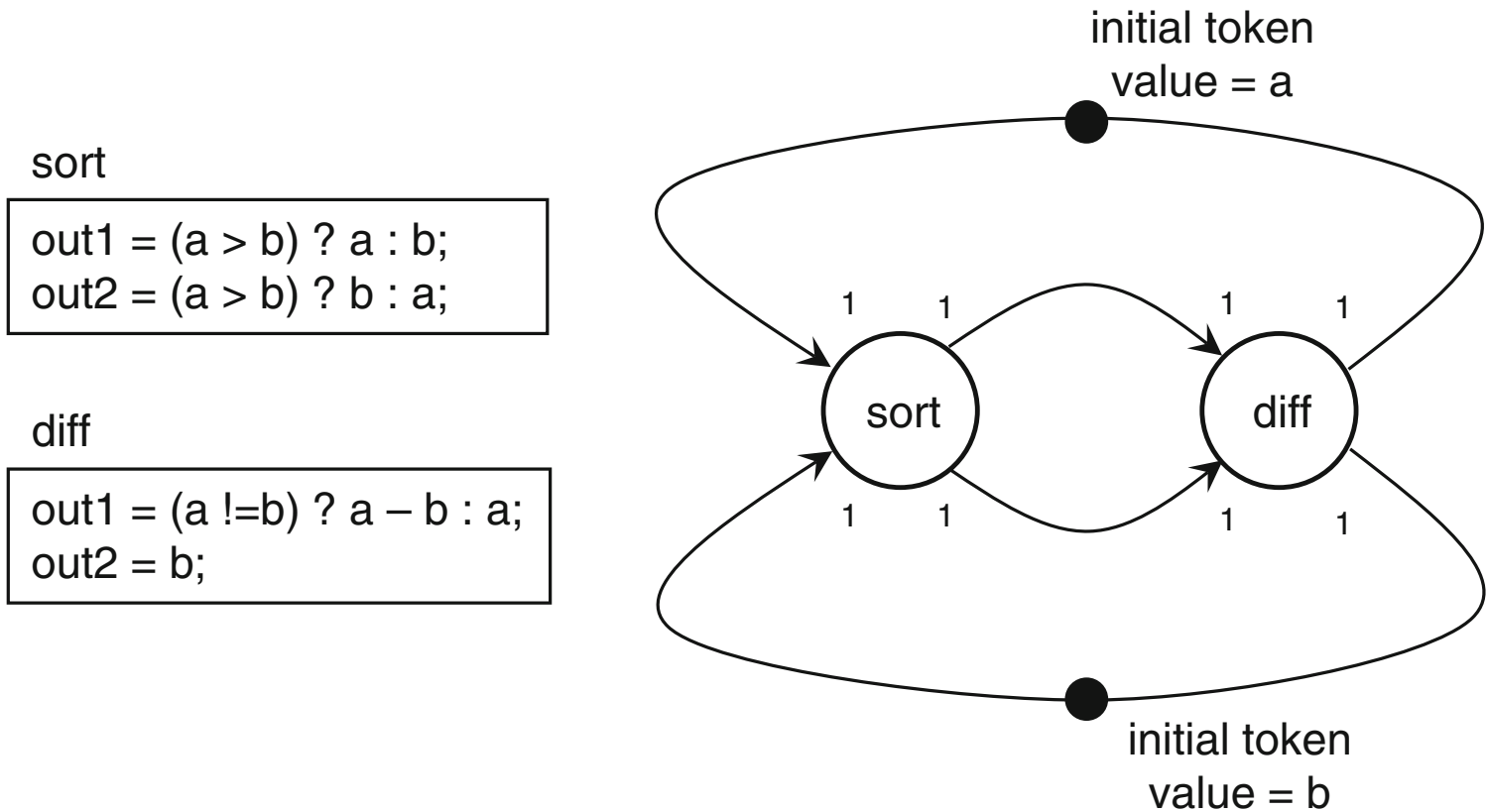


Fig. 3.10 Euclid's greatest common divisor as an SDF graph

Single-Rate SDF to Hardware

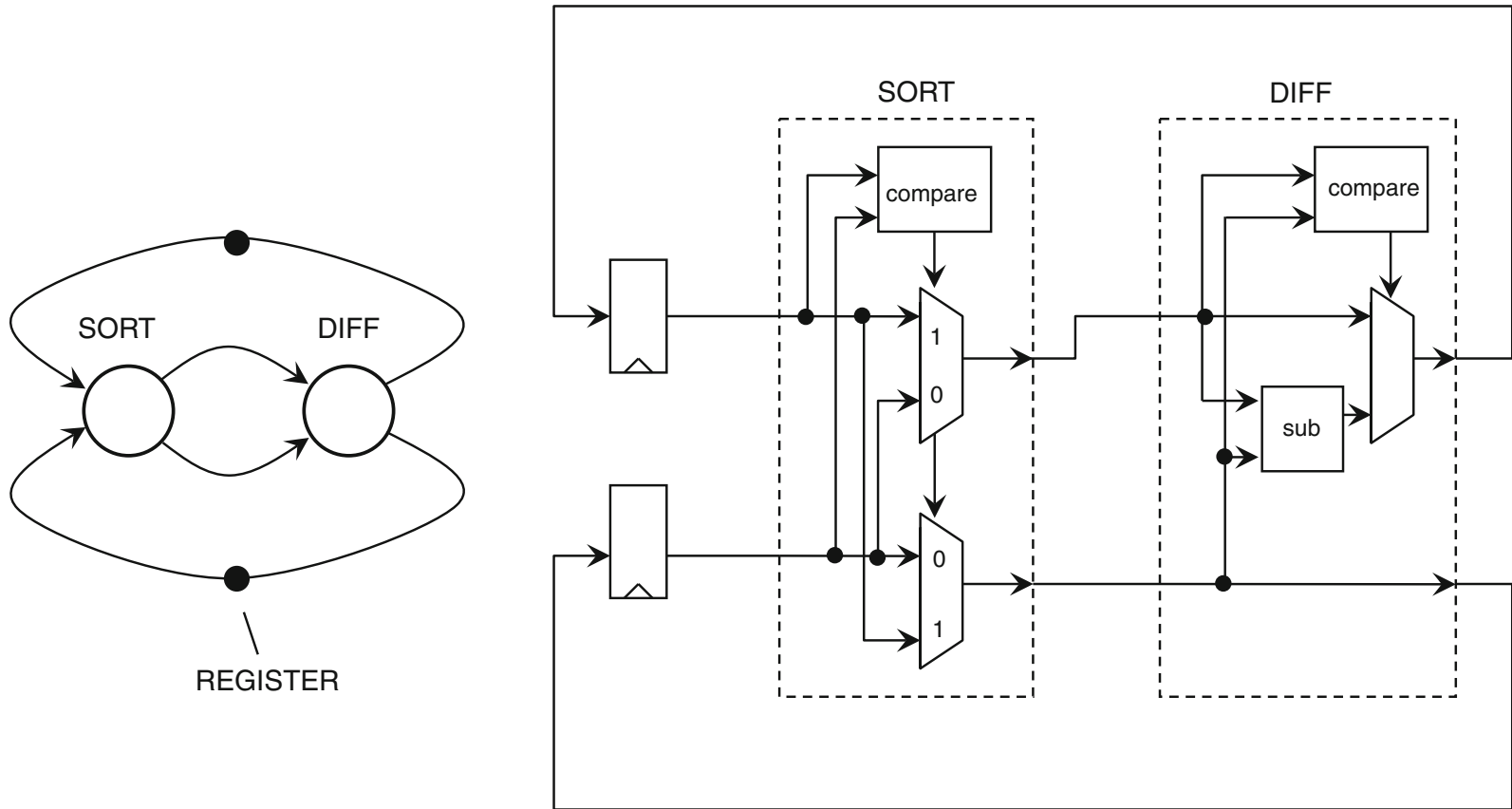


Fig. 3.11 Hardware implementation of euclid's algorithm

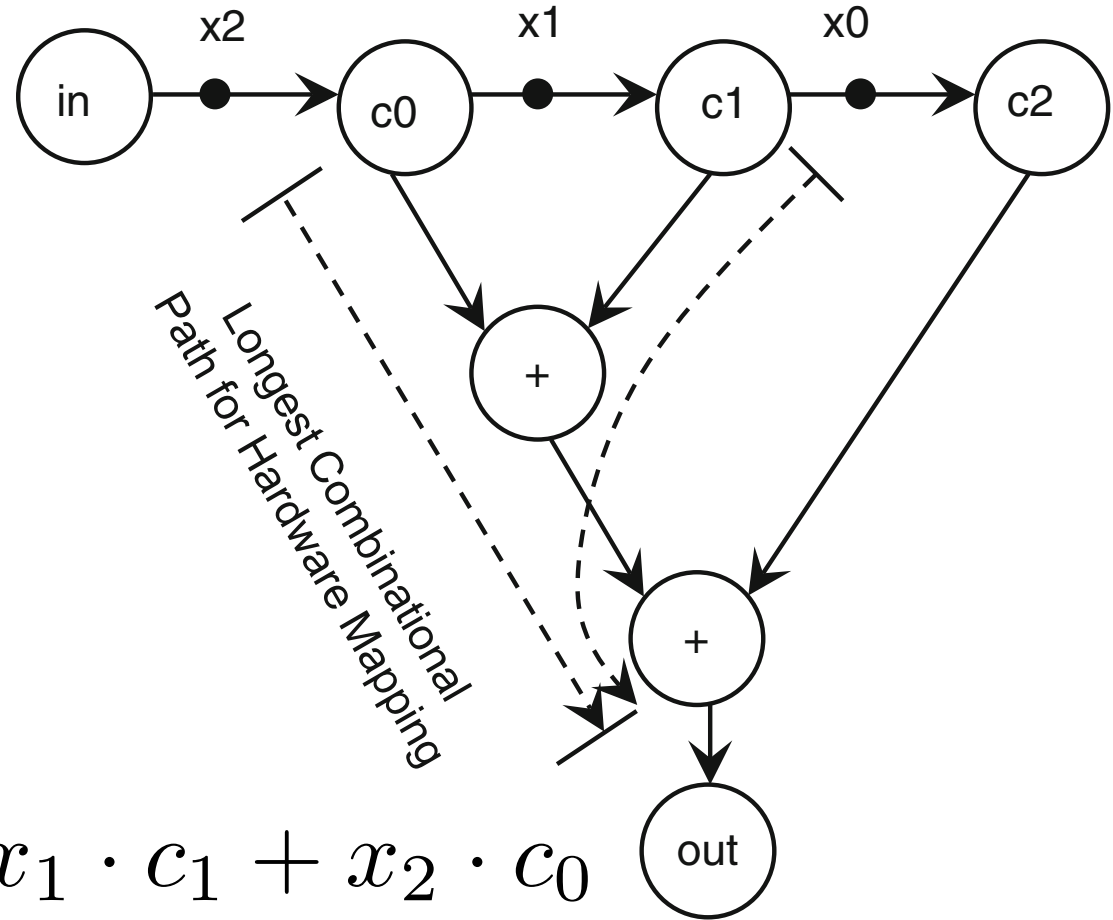
Can lead to **long combination paths.**

SDF HW Implementation

- **Combinational path** is a sequence of actors s.t. edges between these actors do not have initial token.
- **Critical path** is a combinational path s.t. the sum of latencies of all actors on that path is the longest.
- Critical path delay determines the clock frequency.
 - Should be minimized to increase clock speed.

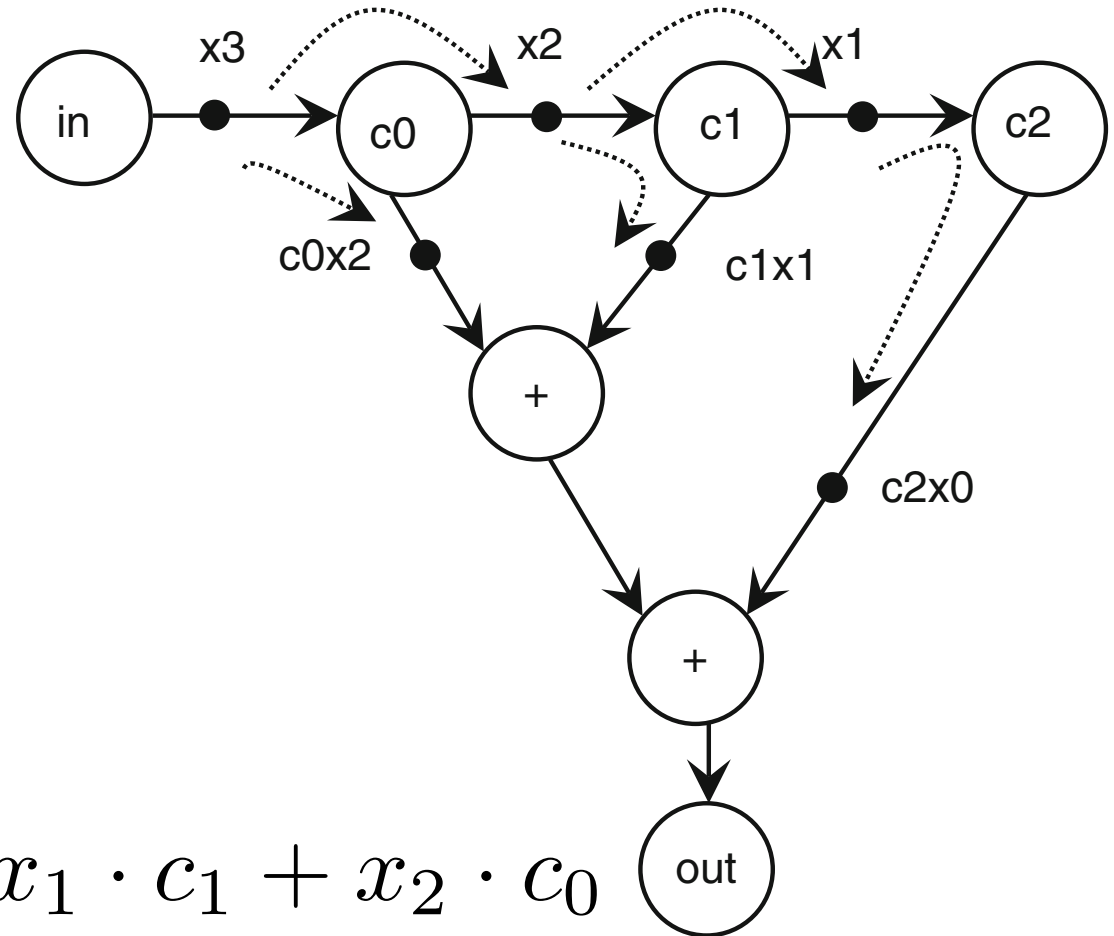
Pipelining: Break Long Comb. Paths

Fig. 3.12 SDF graph of a simple moving-average application



Pipelining: Break Long Comb. Paths

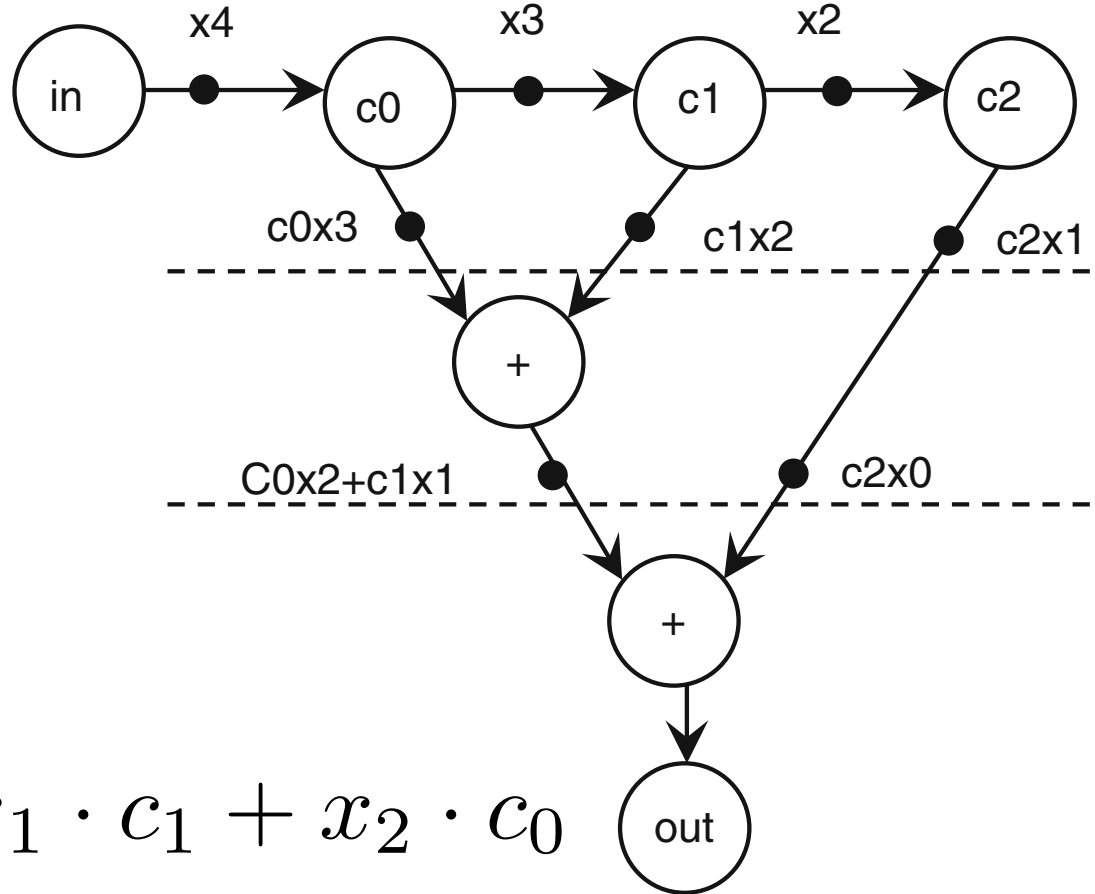
Fig. 3.13 Pipelining the moving-average filter by inserting additional tokens (1)



$$out = x_0 \cdot c_2 + x_1 \cdot c_1 + x_2 \cdot c_0$$

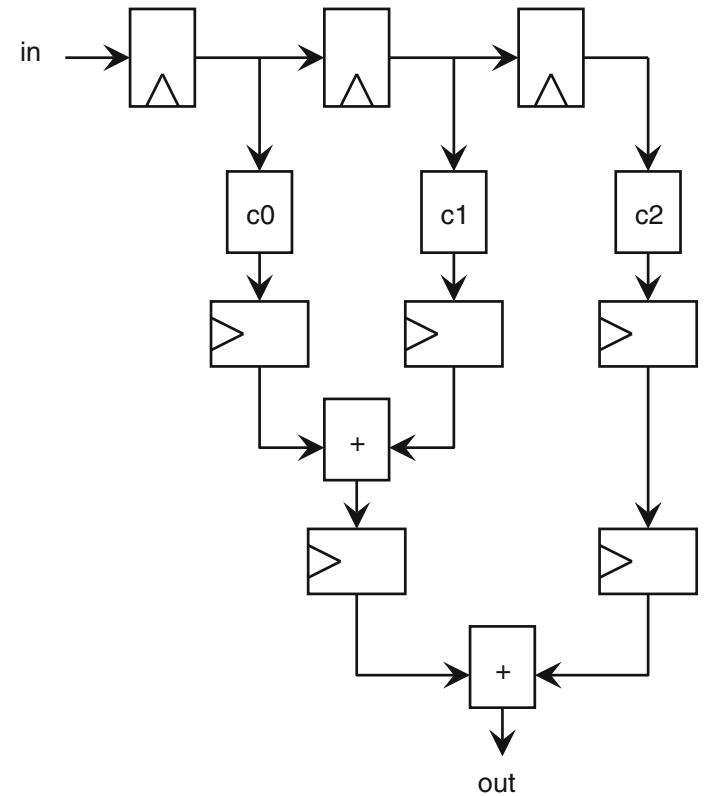
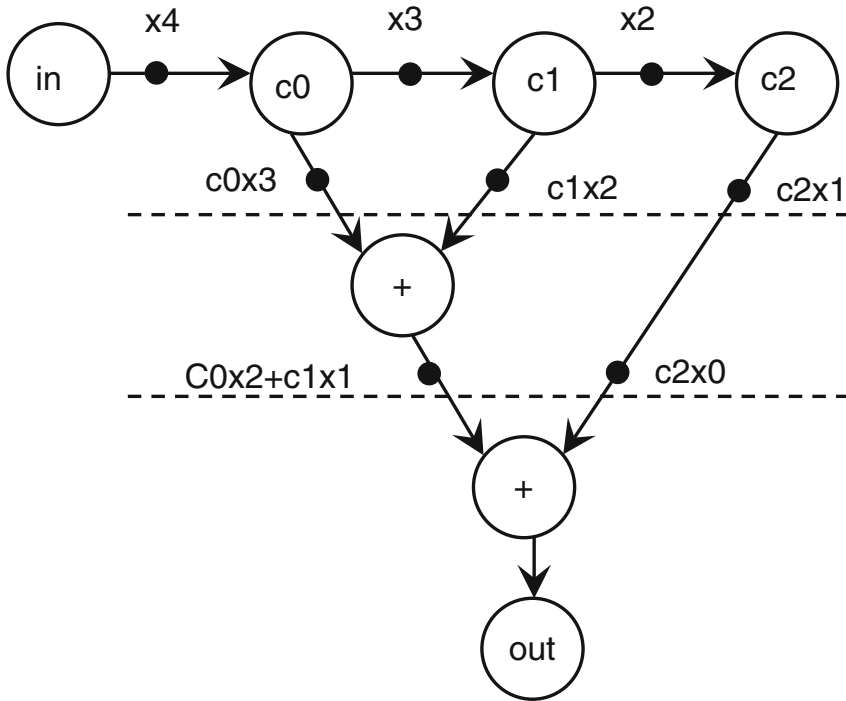
Pipelining: Break Long Comb. Paths

Fig. 3.14 Pipelining the moving-average filter by inserting additional tokens (2)

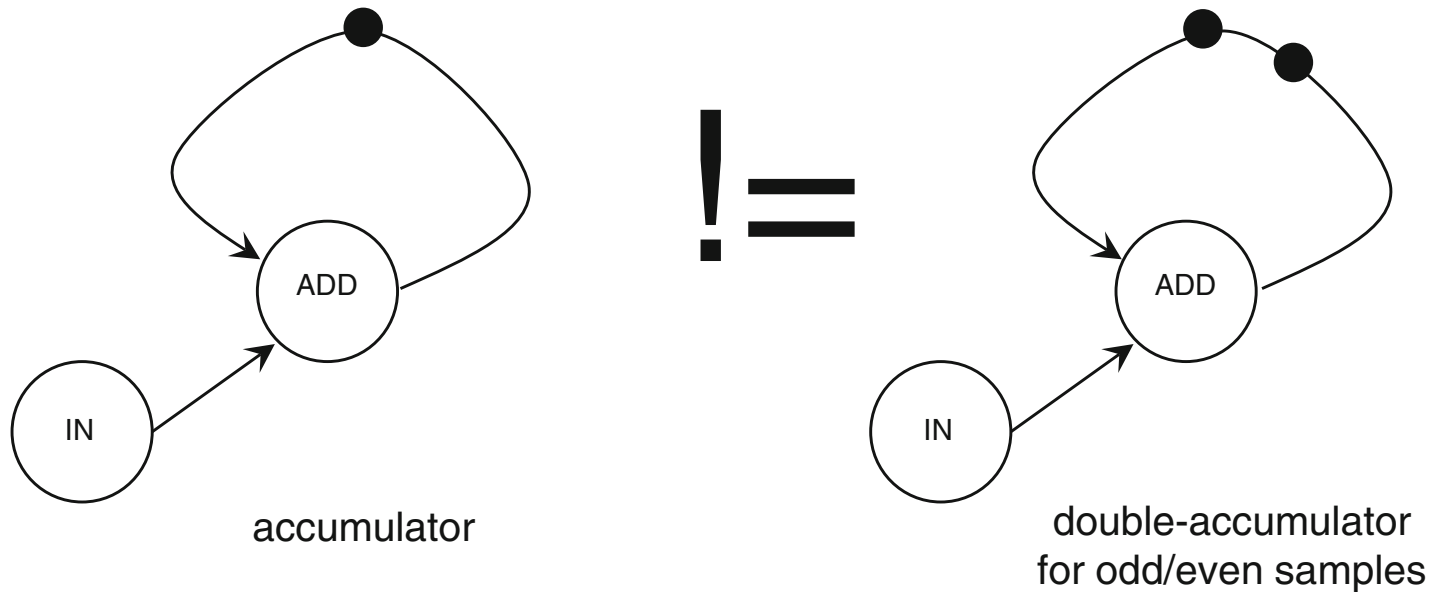


$$out = x_0 \cdot c_2 + x_1 \cdot c_1 + x_2 \cdot c_0$$

Pipelining: Break Long Comb. Paths

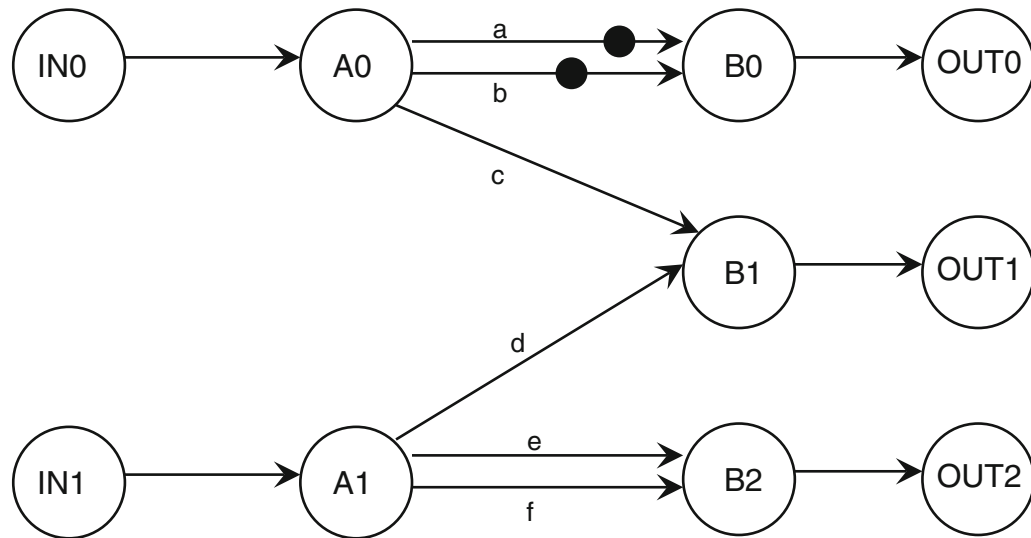
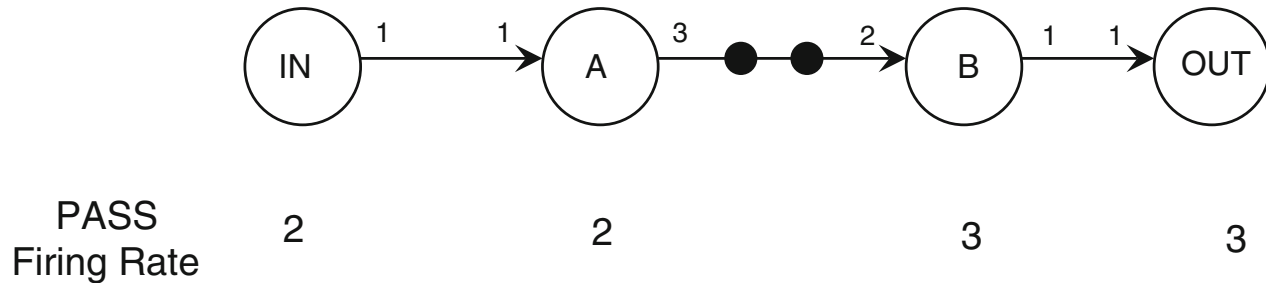


Pipelining: Pitfall



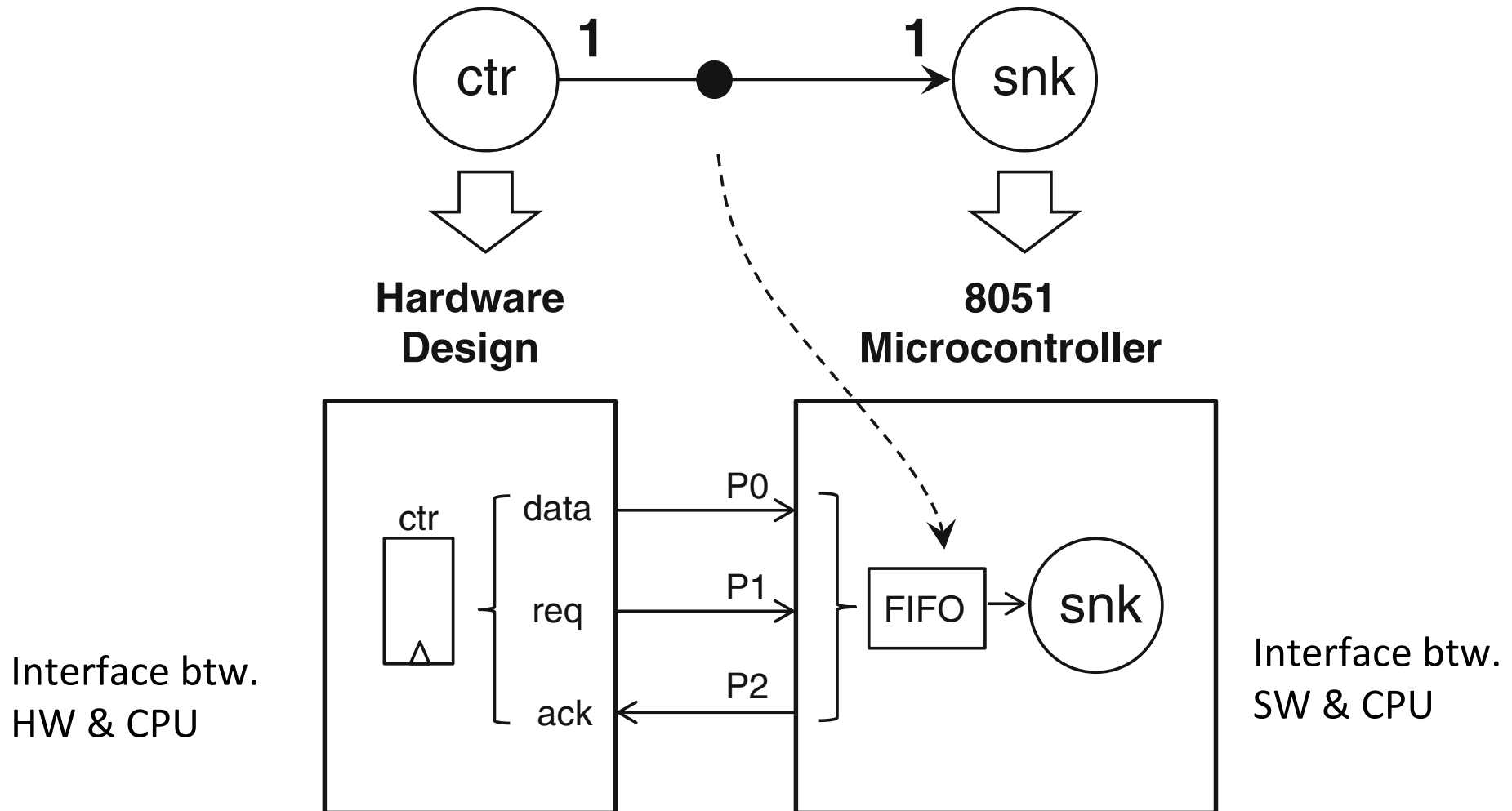
Do **Not** add initial tokens unless they can be injected by a sequence of actor firings.

Multi-Rate Expansion (Sec. 2.5.1)



This single-rate DFG can be mapped to HW as shown previously.

HW/SW Hybrid Implementation



Reading Guide

- Section 3.2 - 3.3, the *CoDesign* book.