CIS 4930 Digital Circuit Testing
Design For Testability

Dr. Hao Zheng
Comp Sci & Eng
Univ of South Florida

Introduction

- Testing cost
  - Test gen., fault sim., test equipment, test process (fault detection and location), etc
- Testing should be considering during the design process
  - enhances “testability” & design quality
  - reduces test cost
- Test complexity determined by three factors
  - Controllability
  - Observability
  - Predictability – ability to obtain know outputs
- *Design for Testability (DFT)* techniques are design efforts to ensure that a device is testable

Introduction

- Testing cost
  - Test gen., fault sim., test equipment, test process (fault detection and location), etc
- Testing should be considering during the design process
- **Design for testability** (DFT) modifies design to
  - enhances “testability” & design quality
  - reduces test cost
- Testability involves
  - **Controllability**
  - **Observability**
  - **Predictability** – ability to obtain know outputs

Testability - Controllability

- **Controllability**
  - ability to establish a specific signal value at each node in the circuit by setting values on PIs
- Circuits difficult to control:
  - Decoders
  - Circuits with feedback
  - Oscillators
  - Clock generators
  - Counters (eg., 16 bit counter, how clock cycles will it take to force MSB to 1?)

Testability - Observability

- **Observability**
  - Ability to determine the signal value at any node in a circuit by controlling circuit's inputs and observing its outputs
- Circuits difficult to observe:
  - Sequential circuits
  - Circuits with global feedback
  - Embedded RAMs, ROMs, or PLAs
  - Circuits with redundant nodes

Some General Observations

- Sequential logic is more difficult to test than combinational logic
- Control logic is more difficult to test than data-path logic
- Random logic is more difficult to test than structured, bus-oriented designs
- Asynchronous designs is more difficult to test than synchronous designs

Tradeoffs

- DFT techniques often reduce costs to test.
  - Improved controllability and observability.
  - Reduced test time, test generation cost,
  - improved test quality -> product quality
- At meantime, they increase product cost.
  - Silicon area, I/O pins, power consumption, and circuit delay.
- Need to balance gain from DFT and its cost

Ad Hoc DFT Techniques

1. Test Points
2. Initialization
3. Monostable multivibrators (one-shots)
4. Oscillators and clocks
5. Counters/Shift Registers
6. Partitioning Large Circuits
7. Logical Redundancy
8. Breaking Global Feedback Paths

1 – Test Points

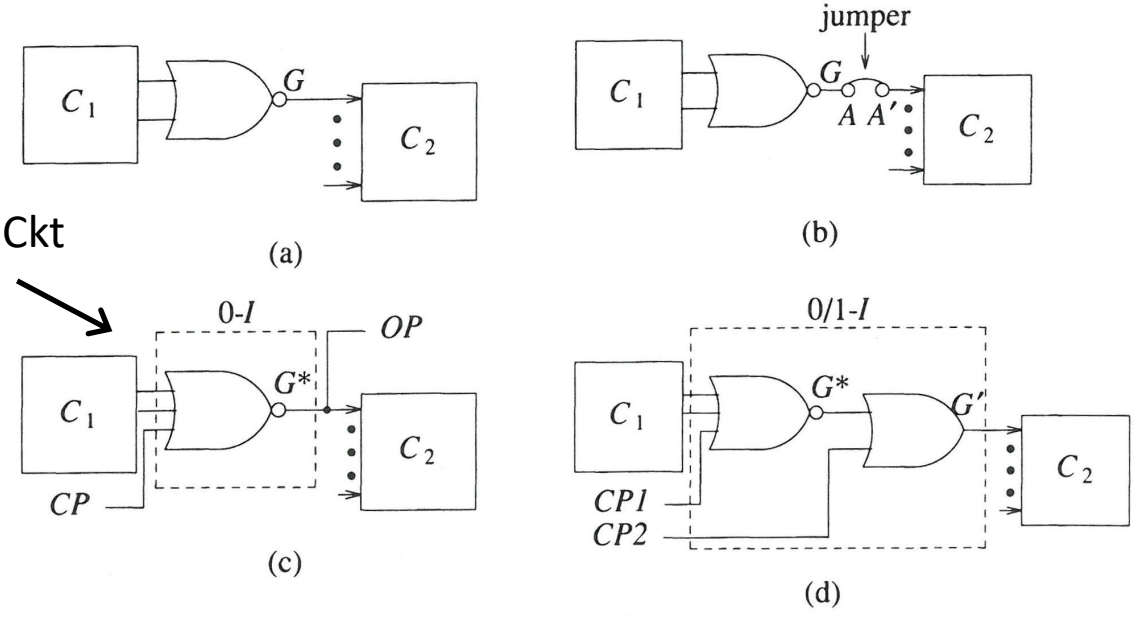
Employ test points to enhance controllability and observability

Two types of test points:

- Control points (CP) = PIs used to enhance controllability
- Observation points (OP) = POs used to enhance observability

Employing Test Points

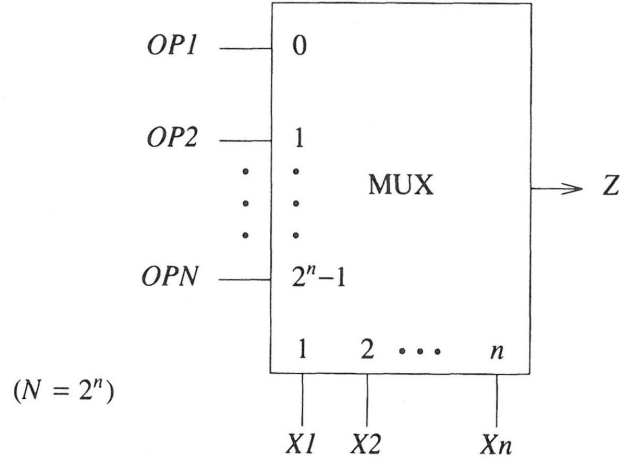
A is an OP
A' is a CP



Demand of large # of IO pins!

Multiplexing Monitor Points

- For limited IO pins, we can use multiplexer
- Drawback – can monitor only one OP at a time -> increases test time
- Select lines can be driven by a counter

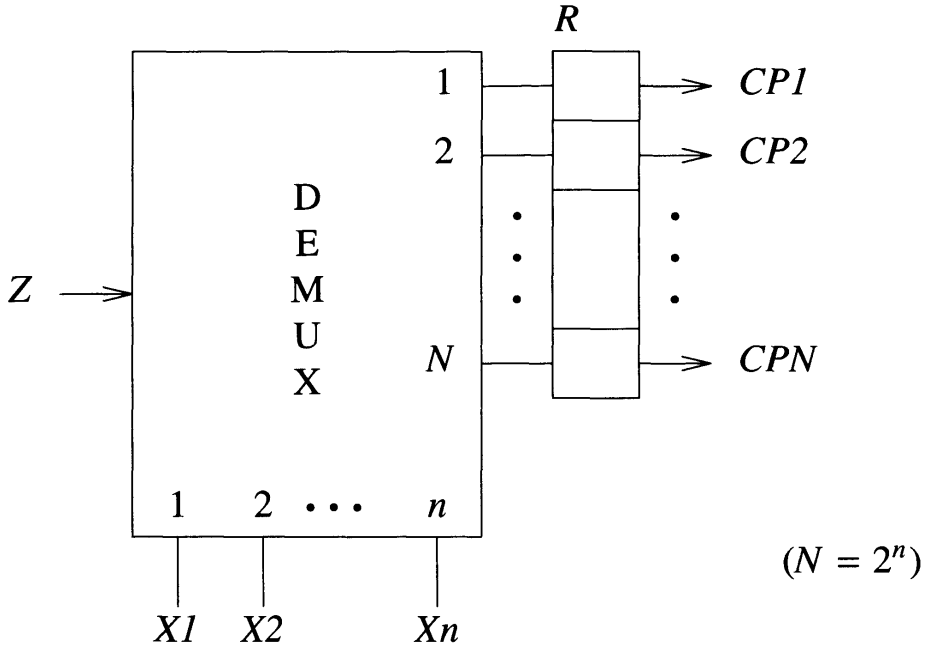


Tradeoff between test time and IO pins.

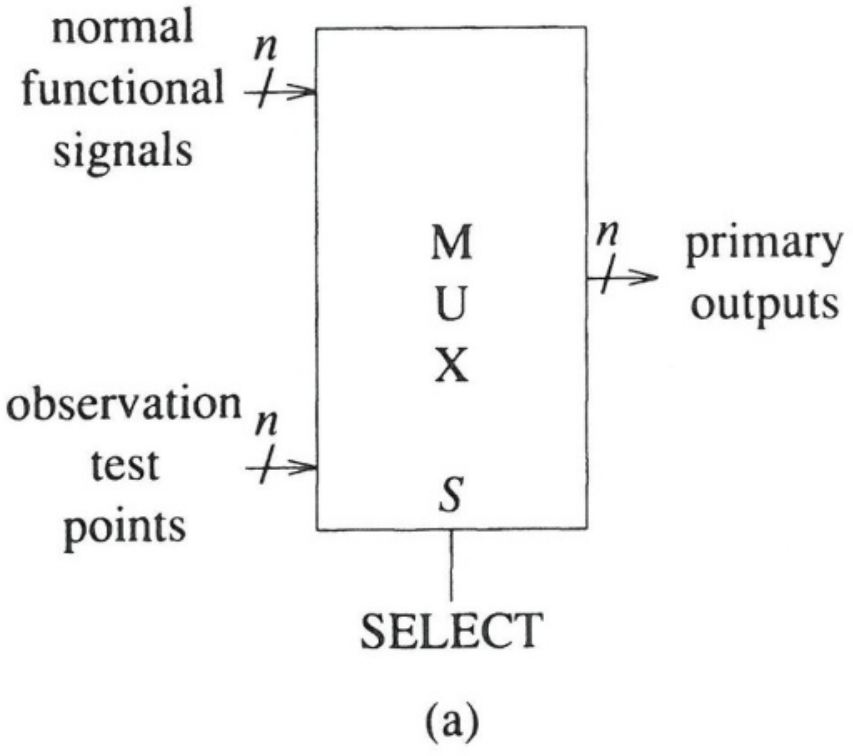
N clock cycles are required between test vectors

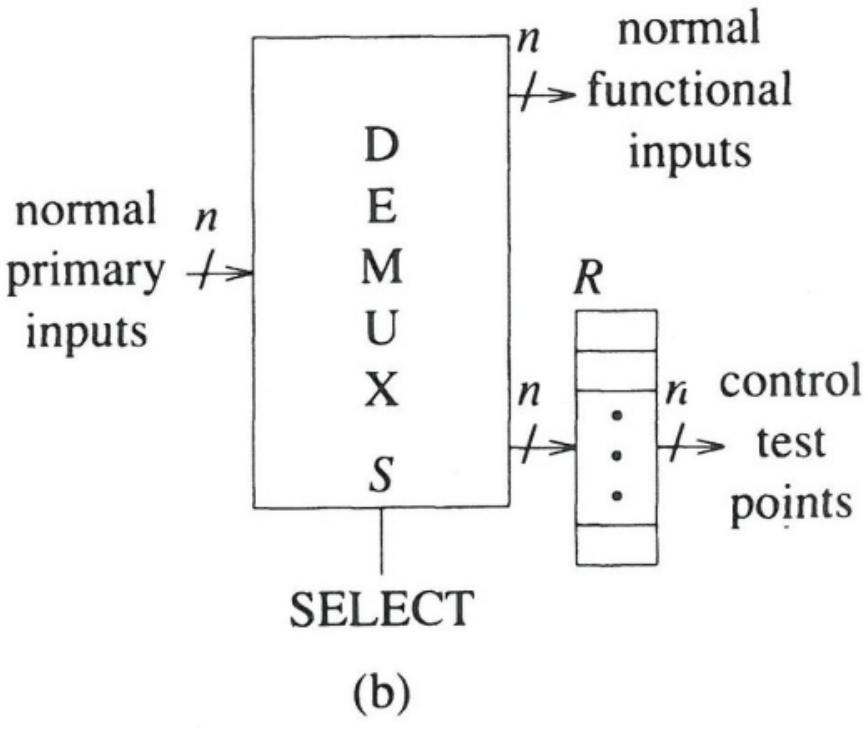
Demux/Latch for Multiple CPs

- Values of 2^n control points are serially applied to input Z
- Stored in N bit-wide latch
- Need *N* cycles to set up the control values



Time-Sharing Normal I/O Pins





Signal Selection – Control Points

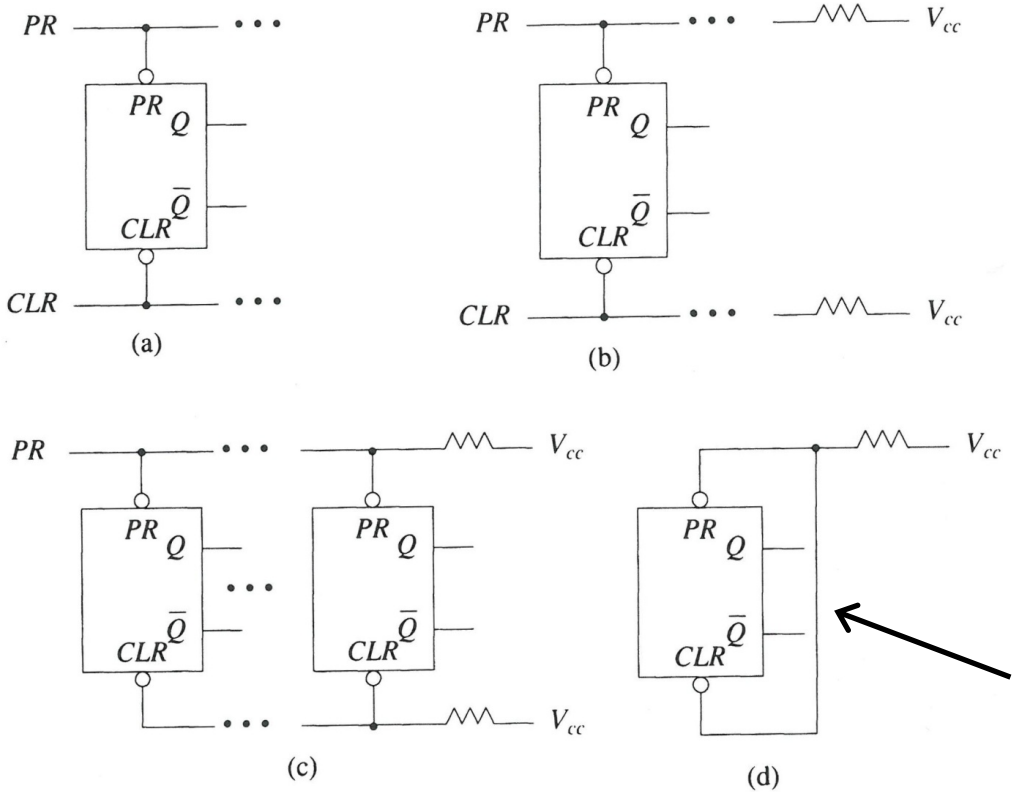
- Control, address, and data bus lines on bus-structured designs
- Enable/hold inputs to microprocessors
- Enable and read/write inputs to memory devices
- Clock and preset/clear inputs to memory devices
- Data select inputs to muxes/demuxes
- Control lines on tri-state devices

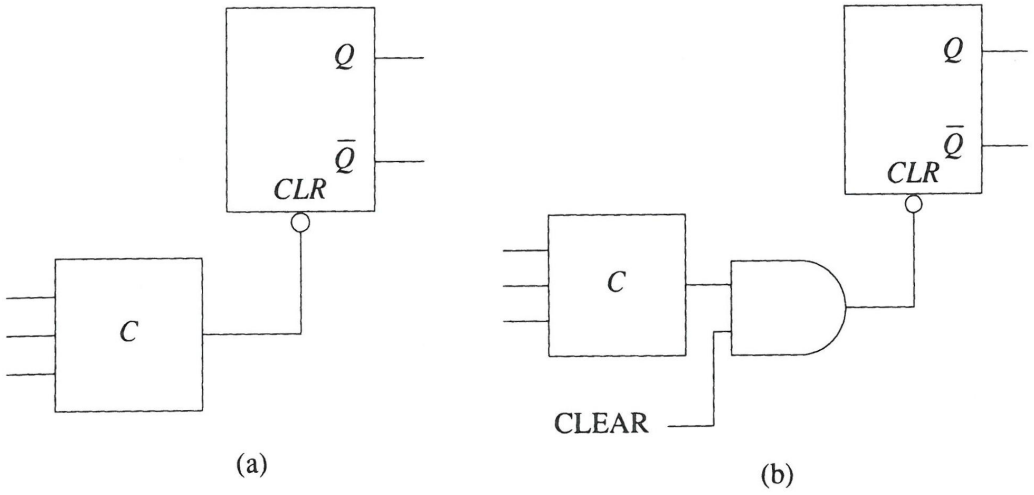
Signal Selection – Observation Points

- Stem lines associated with signals having high fanout
- Global feedback paths
- Redundant signal lines
- Outputs of logic devices having many inputs (muxes, parity generators)
- Outputs from state devices (FFs, Counters, Shift Registers)
- Address, control, and data busses

2 – Initialization

Design circuits to be easily initializable





Set/reset controlled by logic gates

Figure 9.6 (a) Flip-flop without explicit clear (b) Flip-flop with explicit clear

Set/reset signal controlled internally

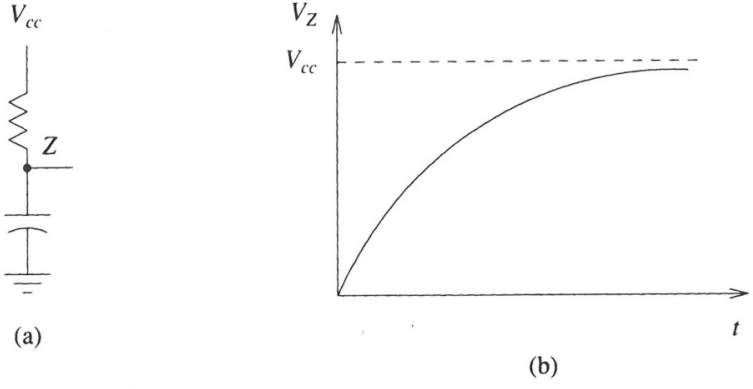
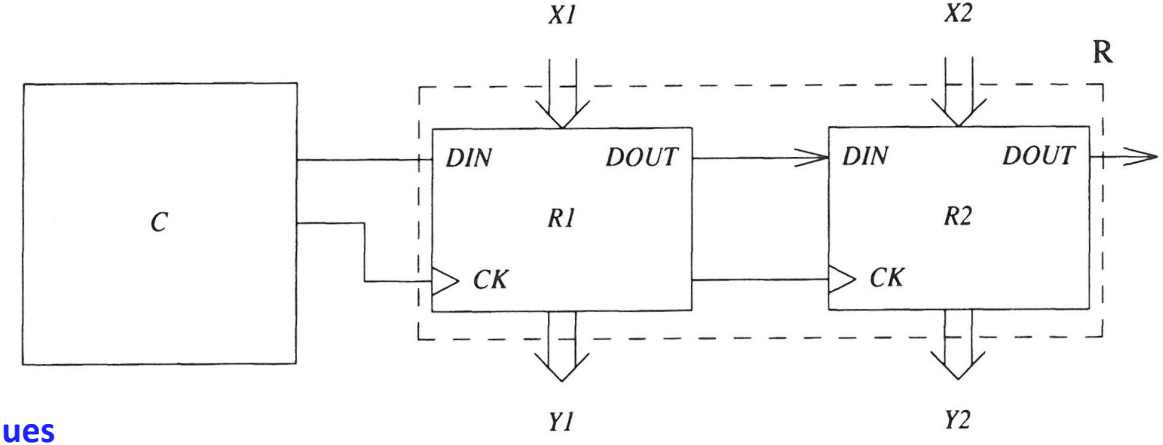


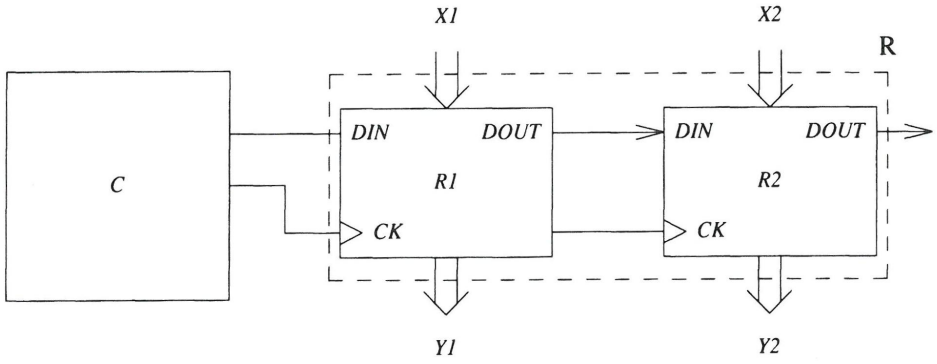
Figure 9.7 Built-in initialization signal generator

5 – Partitioning Counters and Shift Registers

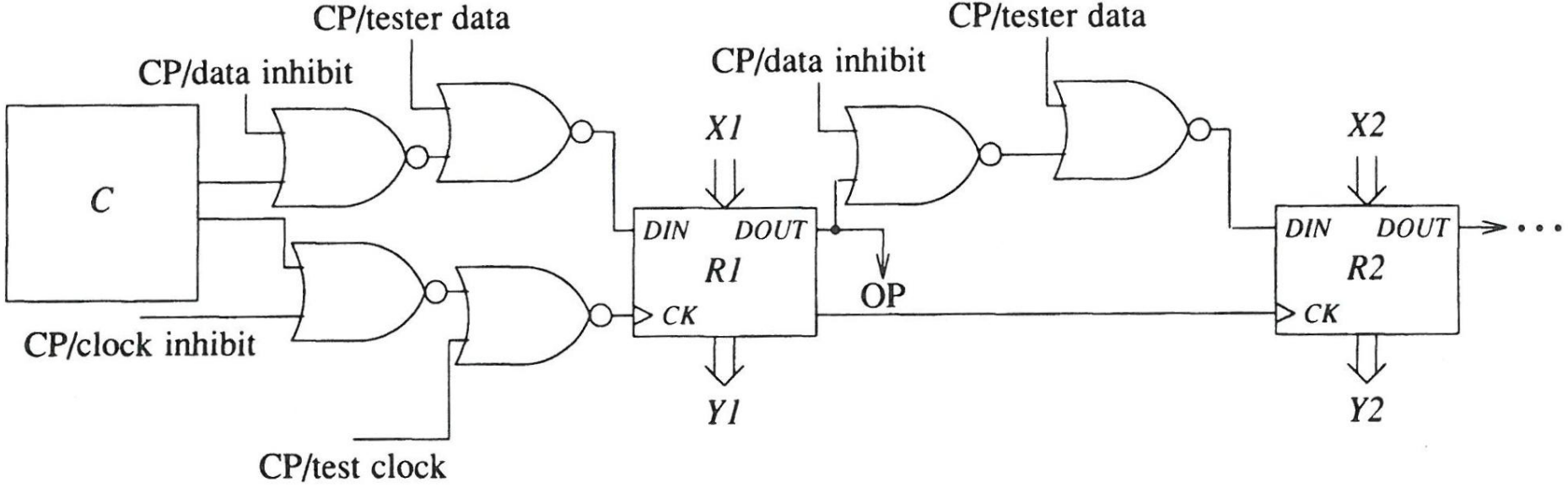
Partition large counters and shift registers into smaller units

- Counters/SR are difficult to test because test sequences usually require many clock cycles
- Partition the register for better control/obs.




X1
X2
R
C
DIN
DOUT
R1
CK
DIN
DOUT
R2
CK
Y1
Y2

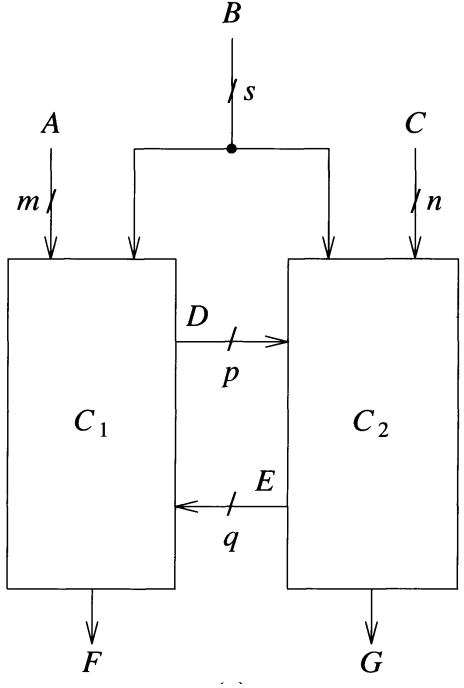
(a)

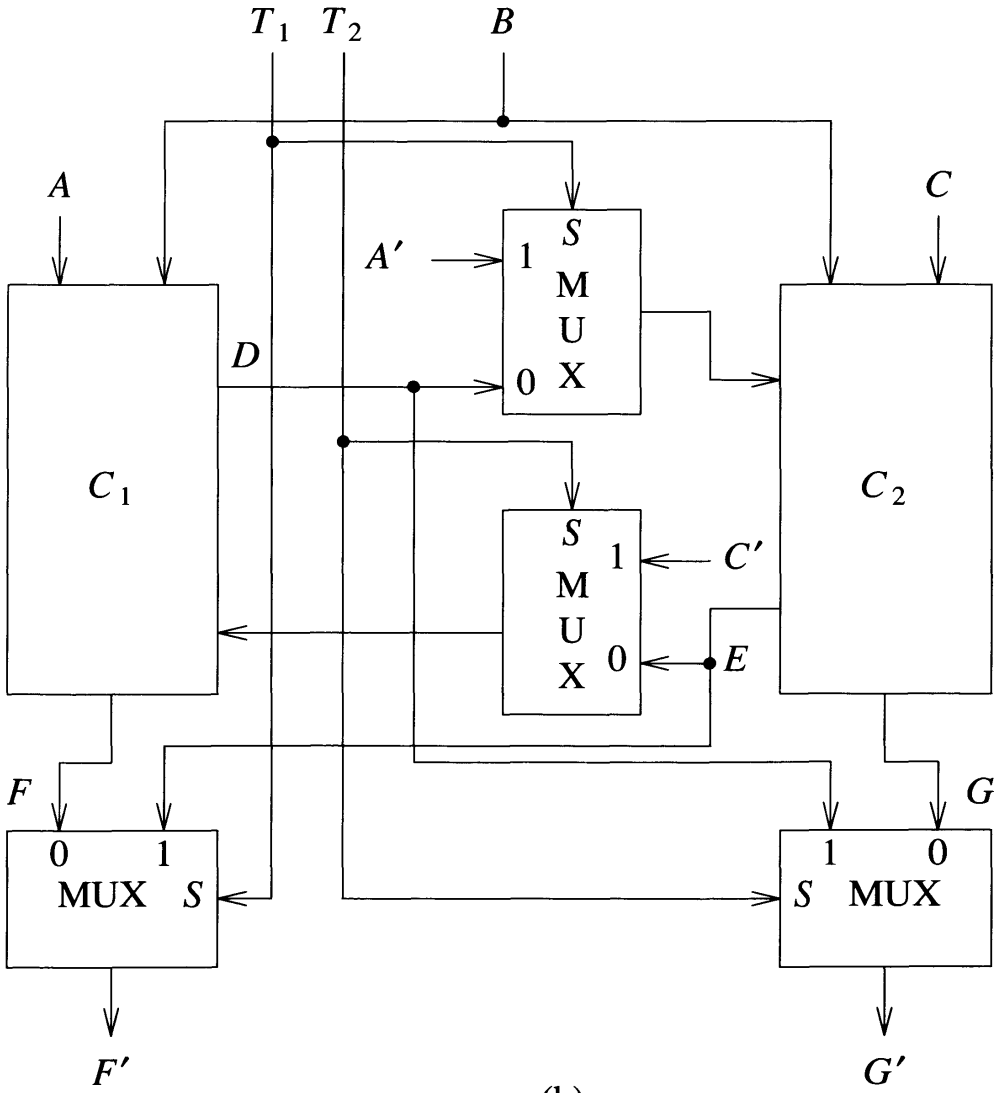

CP/tester data
CP/data inhibit
CP/tester data
CP/data inhibit
X1
X2
C
DIN
DOUT
R1
CK
OP
DIN
DOUT
R2
CK
CP/clock inhibit
Y1
Y2
CP/test clock

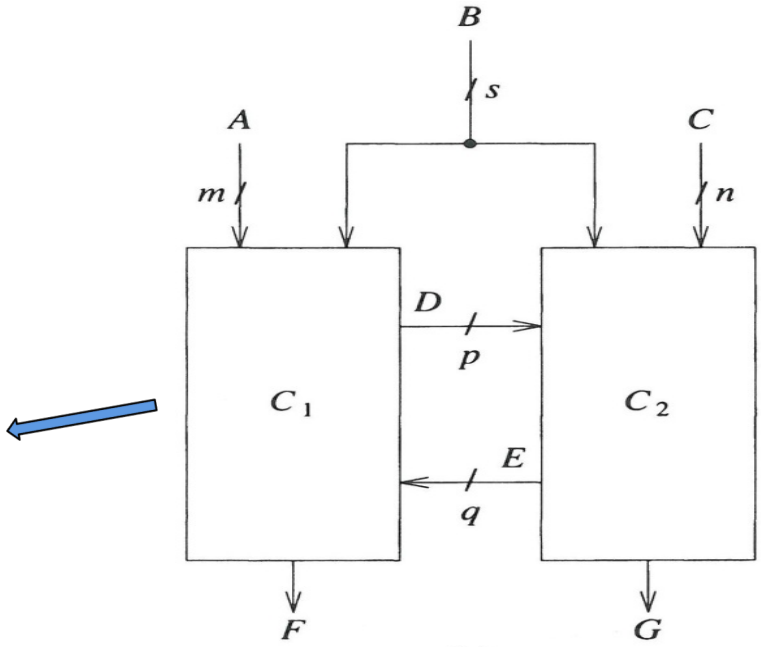
6. Partitioning of Large Comb. Circuits

Partition large circuits into small subcircuits to reduce test generation costs.

- Time complexity ...on grows faster than a linear function of
- Partitioning can r... generation cost







T_1	T_2	Mode
0	0	normal
0	1	test C_1
1	0	test C_2

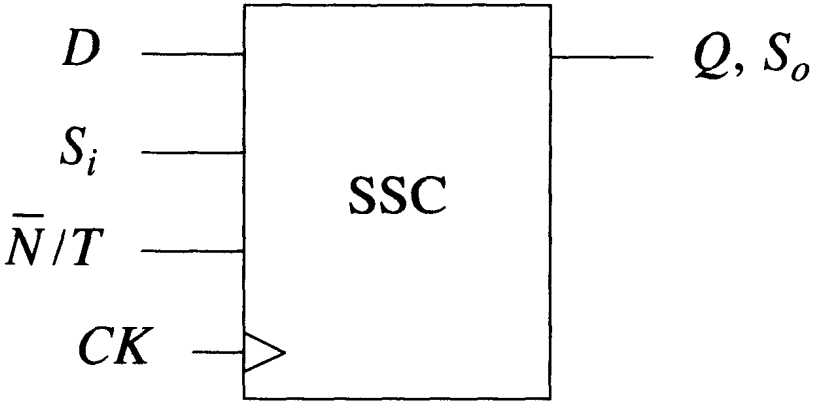
7 – Logical Redundancy

- **Rule:** *Avoid the use of redundant logic.*
- Redundancy makes faults undetectable
- It may invalidate some test for nonredundant faults
- Can cause difficulty in fault coverage calculations
- Redundancy can be introduced inadvertantly
  - Maybe difficult to remove.
  - Test points can be added to remove redundancy during testing

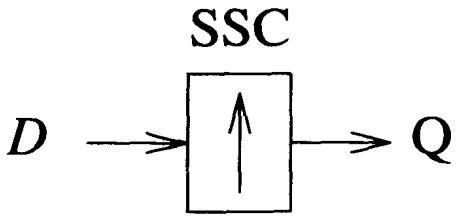
Scan Registers

- Test points are costly in terms of I/O pins
- Scan Register is an alternative – tradeoff between test time, area, and I/O pins
- Scan Register (SR) = Register with both shift and parallel-load capability
- Storage cells in SR can be used as observation and control points

Scan Storage Cell (SSC)



(a)

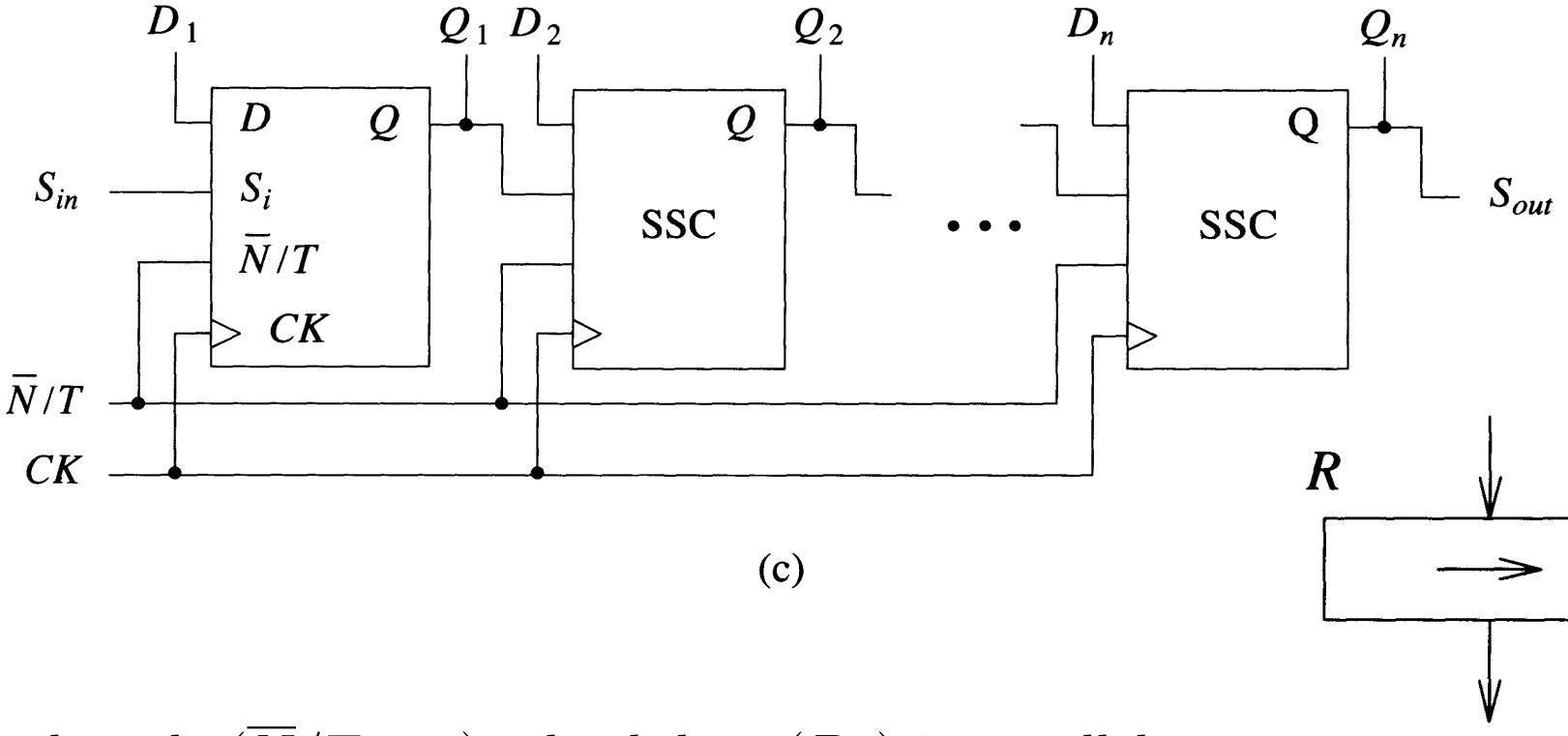


(b)

$\overline{N}/T = 0$ Normal mode: *D* is loaded

$\overline{N}/T = 1$ Testing mode: *S* is loaded

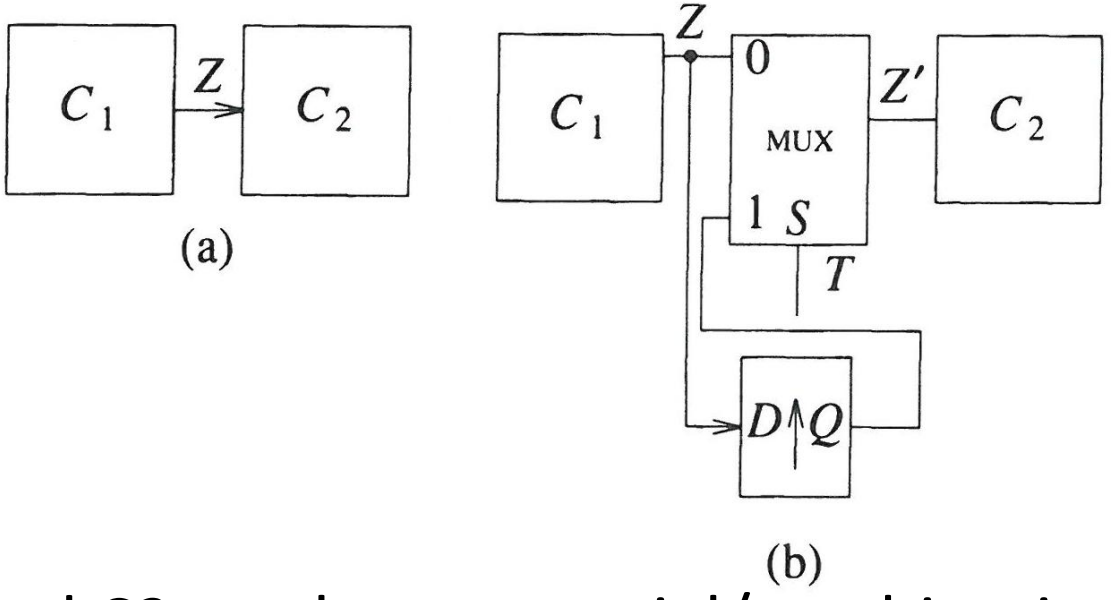
Scan Register



Normal mode ($\overline{N}/T = 0$) load data (D_x) in parallel

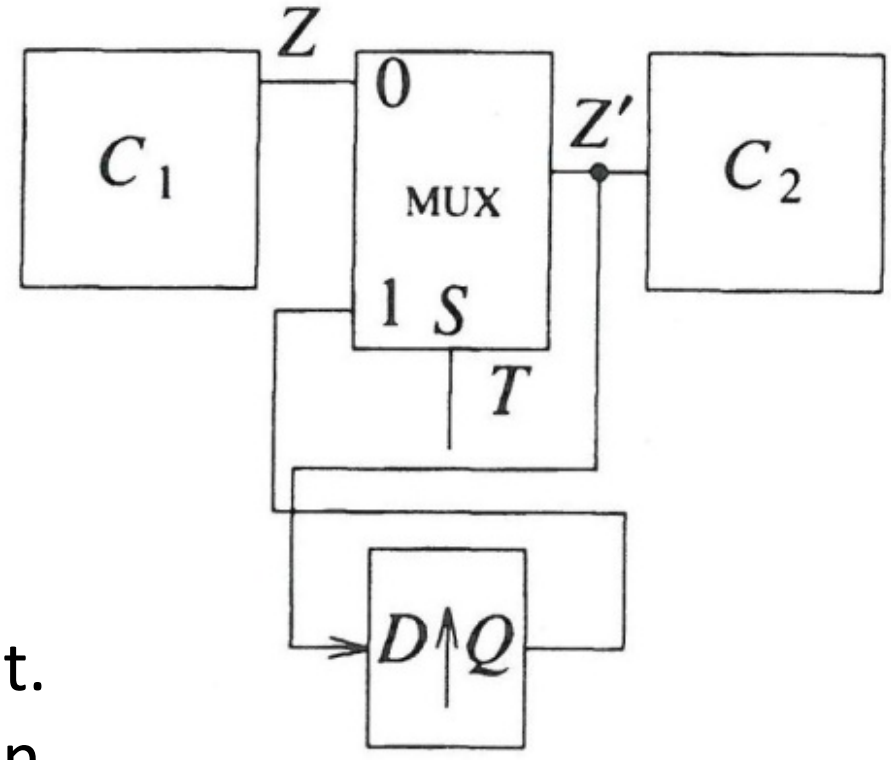
Test mode ($\overline{N}/T = 1$) shift data (from S_{in} to S_{out})

Simultaneous Controllability and Observability



- C1 and C2 can be sequential/combinational
- Z can be loaded into SSC via scan-in and observed by scan-out operation
- Data can be loaded in SSC via *D*-input and injected onto line Z'

Separate Controllability and Observability

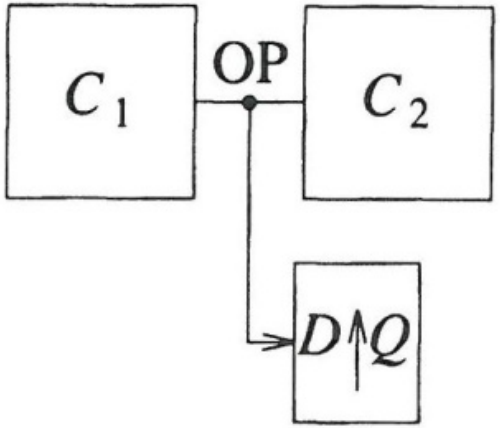


(c)

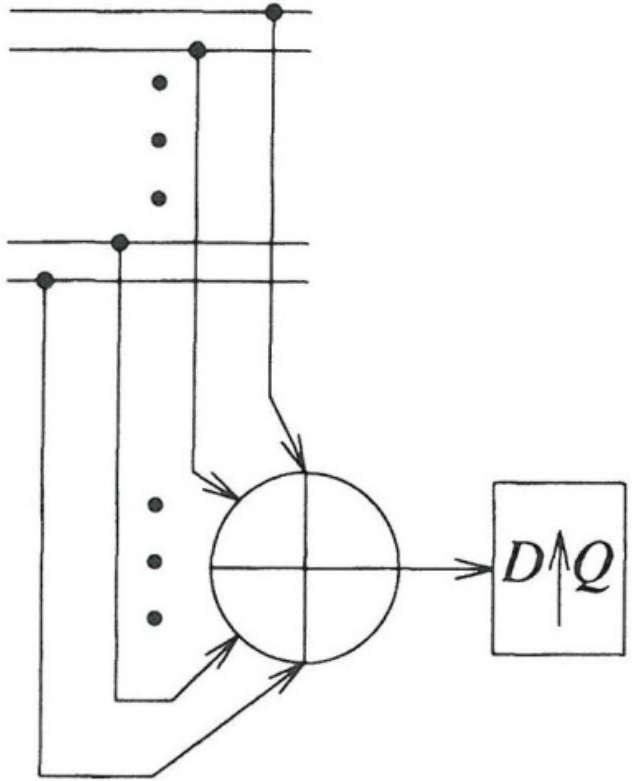
Z' is connected to *D*-input.

CP is connected to Scan-in.

Observability Only

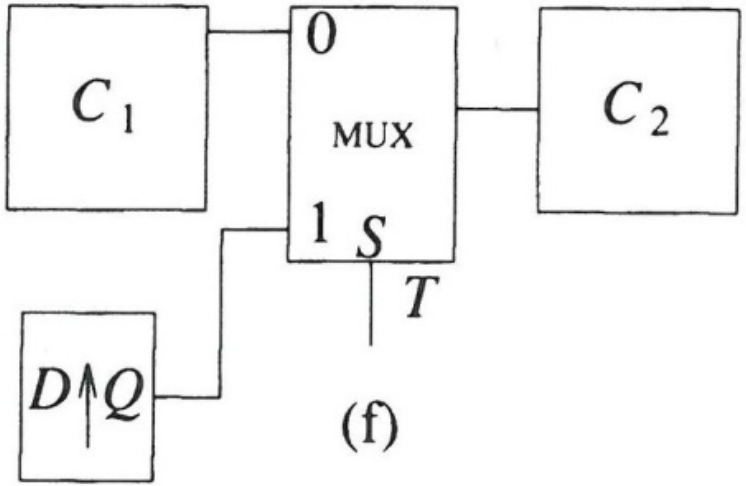


(d)



(e)

Controllability Only



Making Undetectable Faults Detectable

- *X'* = Control points Z' = Observation points
- Lets say *f* is an undetectable fault
- Choose X' and Z' such that *f* becomes detectable
- R1 and R2 can be combined as a single register

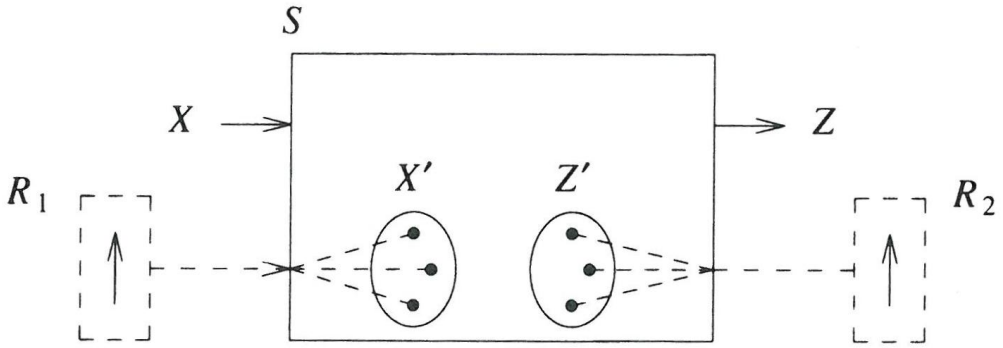
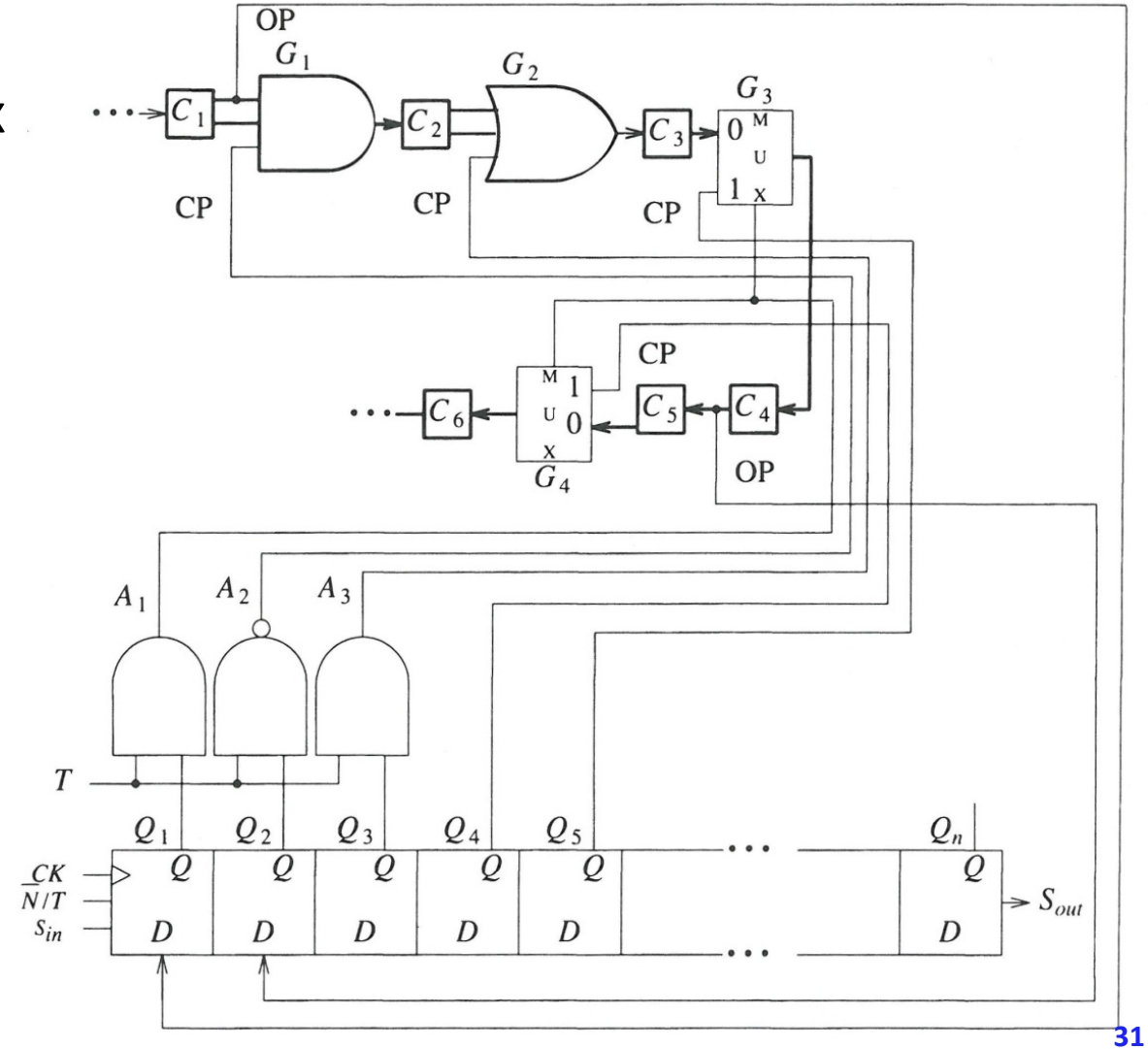


Figure 9.15 General architecture using test points tied to scan registers

Example 1 – Enhancing Testability

- C1, C2, … C6 are Complex Seq/Comb blocks.
- # of CPs and OPs decides the length of scan register.
- *How does it work?*



Generic Scan-Based Designs

- Scan Design – most popular structured DFT technique, employs a scan register
- Several forms of scan designs – differ primarily in the scan cell design
- Three generic forms of scan design
  - Full Serial Integrated Scan
  - Isolated Serial Scan
  - Non-serial Scan

Full Serial Integrated Scan

All storage elements in the design become part of scan register.

Instead of testing circuit in (a) as a sequential circuit, now *C* can be tested using a series of test vectors.

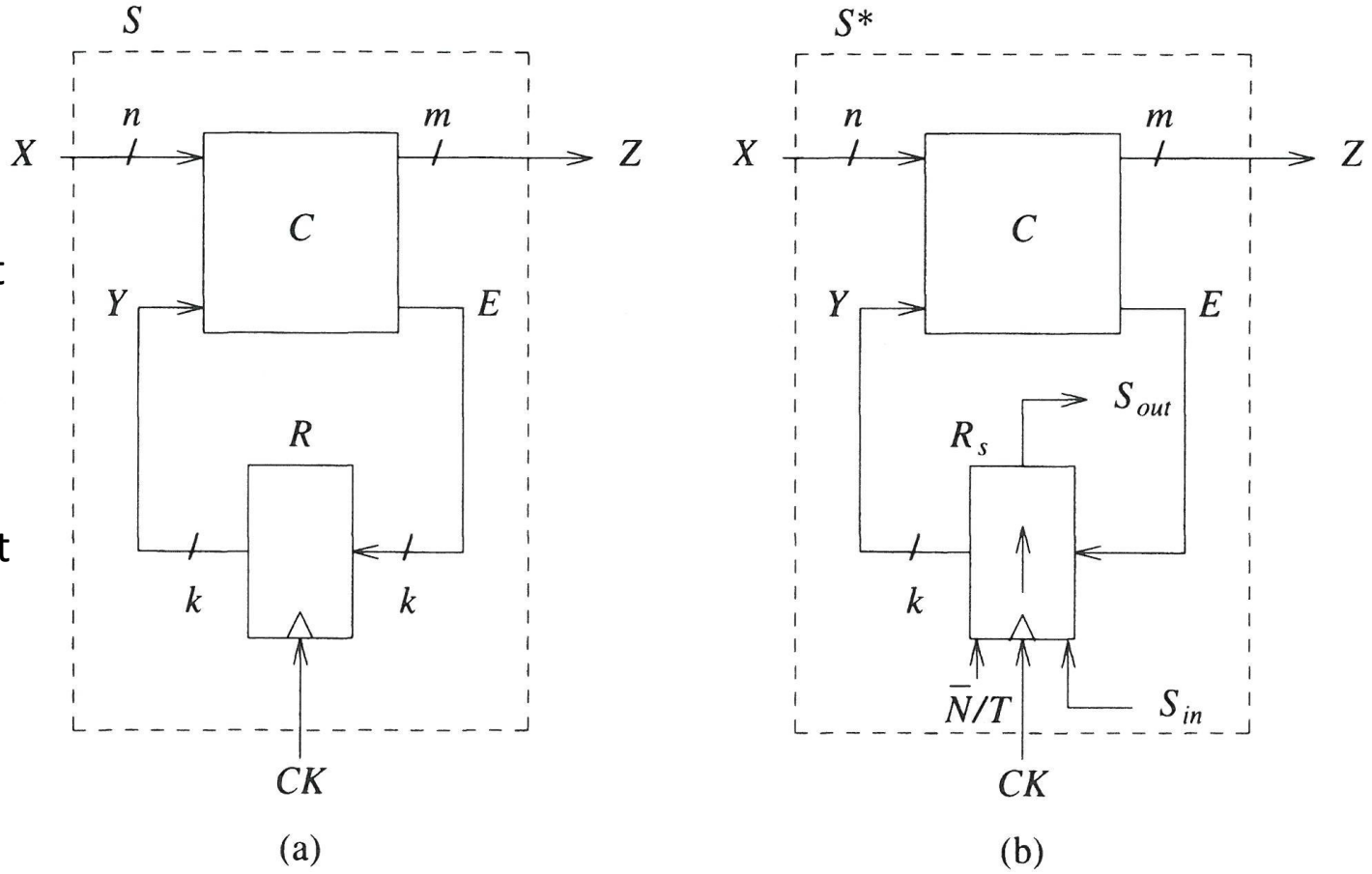


Figure 9.19 (a) Normal sequential circuit *S* (b) Full serial integrated scan

Isolated Serial Scan

- Unlike Full Serial, Scan register is not part of the data path

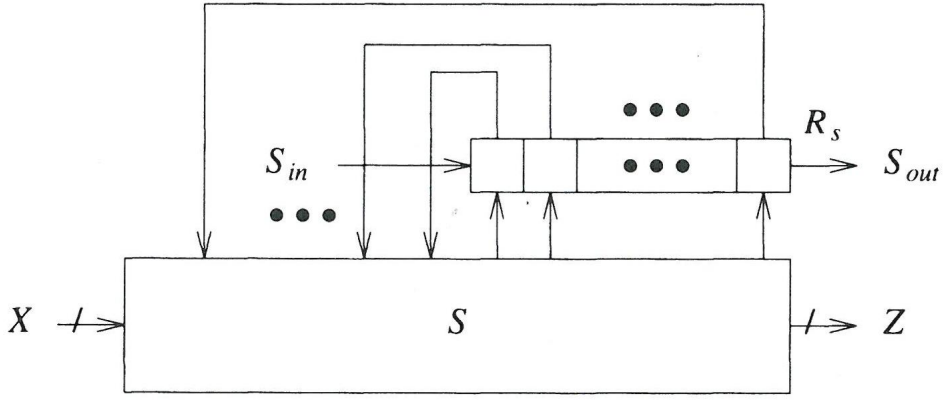


Figure 9.20 Isolated serial scan (scan/set)

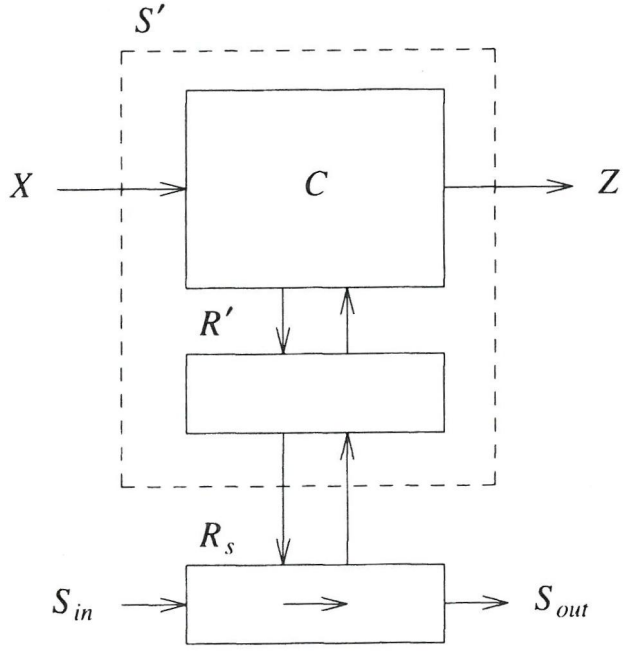


Figure 9.21 Full isolated scan

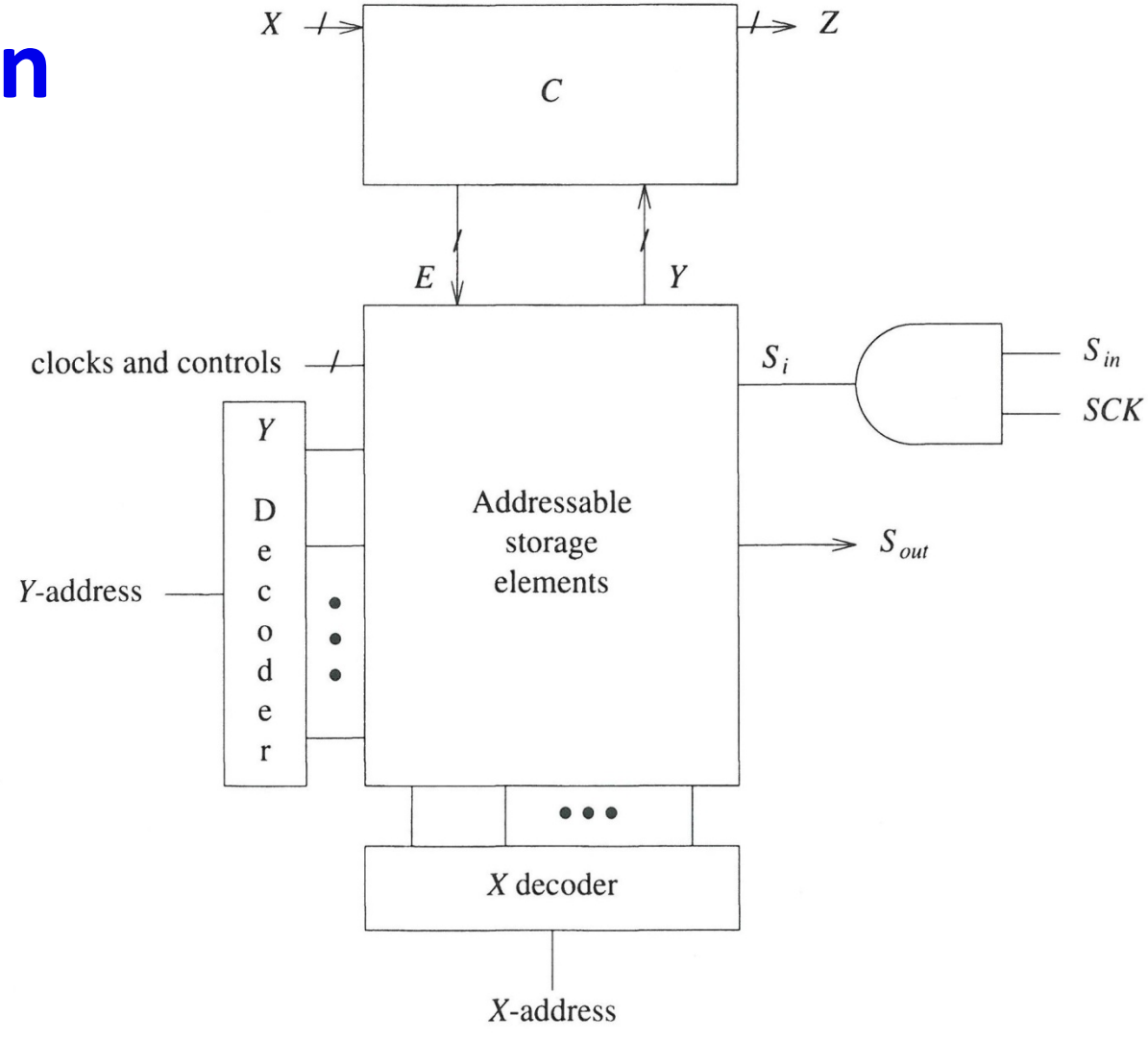
Shadow register R_s: does not interfere the normal operation,

Non-Serial Scan

RAM is used instead of shift register.

Individual bits can be modified for selected CPs or OPs.

Area overhead is high.



Generic Boundary Scan

- Concept – in designing modules such as complex chips or PCBs, for local testing and fault isolation, we should be able to isolate one module from another
- All chips on board are designed using boundary scan architecture
- Boundary scan registers are on the periphery; not part of the function
- Test vectors can be scanned in and responses saved and scanned out
- Internal clock must be disabled

Generic Boundary Scan

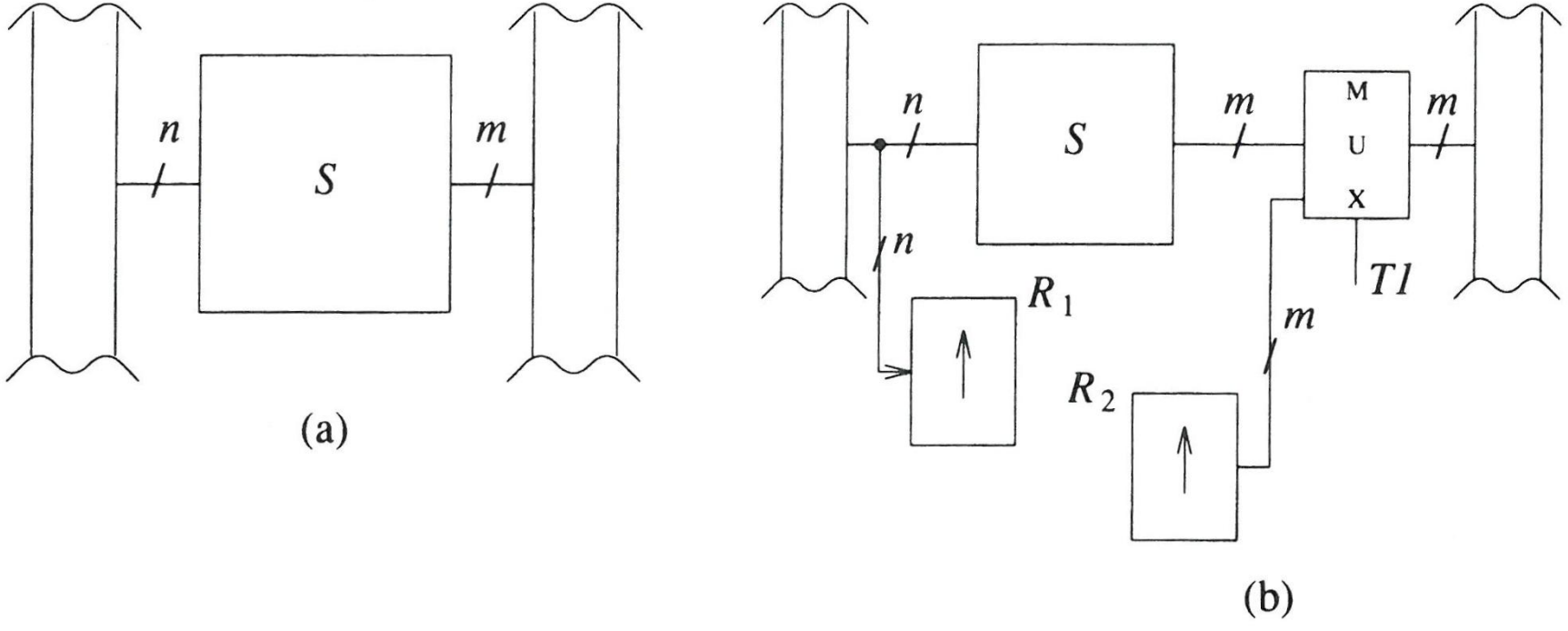


Figure 9.18 Boundary scan architecture (a) Original circuit (b) Modified circuit

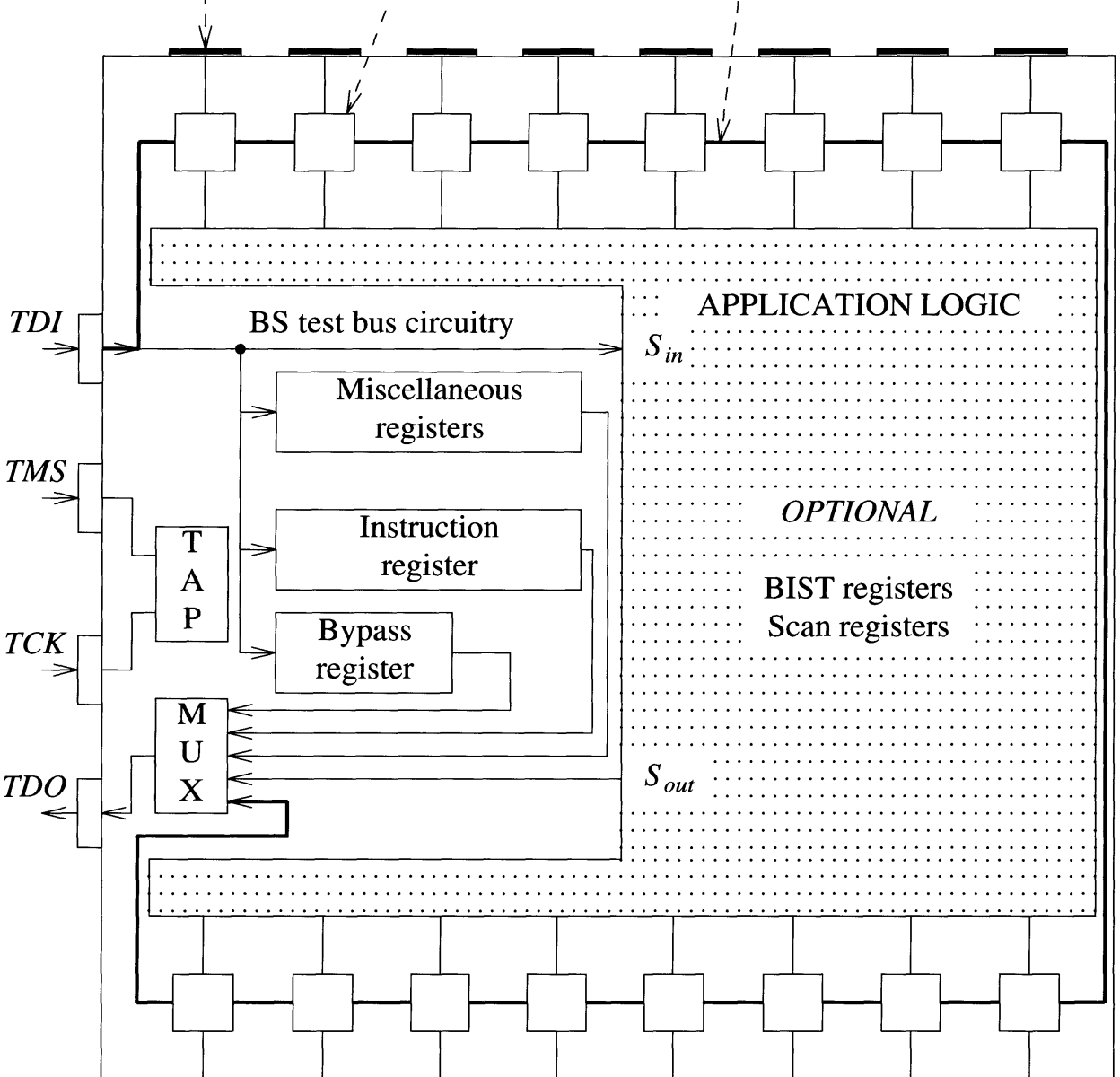
Boundary-Scan Standards

- Goal – to ensure chips of VLSI complexity contain standard DFT circuitry to make test development effective and less costly
- Some initiatives
  - Joint Test Action Group (JTAG) Boundary Scan Std
  - VHSIC Element Test and Maintenance (IBM Std)
  - IEEE 1149.1 Testability Bus Standard
- Primarily deal with
  - Test Bus (resides on the board)
  - Bus Protocol
  - Interface logic between test bus ports and DFT hardware
- JTAG Boundary Scan and IEEE 1149.1 require a bound-scan register exist on the chip

TAP = Test Access Port

- TDI = Test Data Input
- TDO = Test Data Output
- TMS = Test Mode Signal
- TCK = Test Clock

TAP Controller = a FSM control operation of test bus

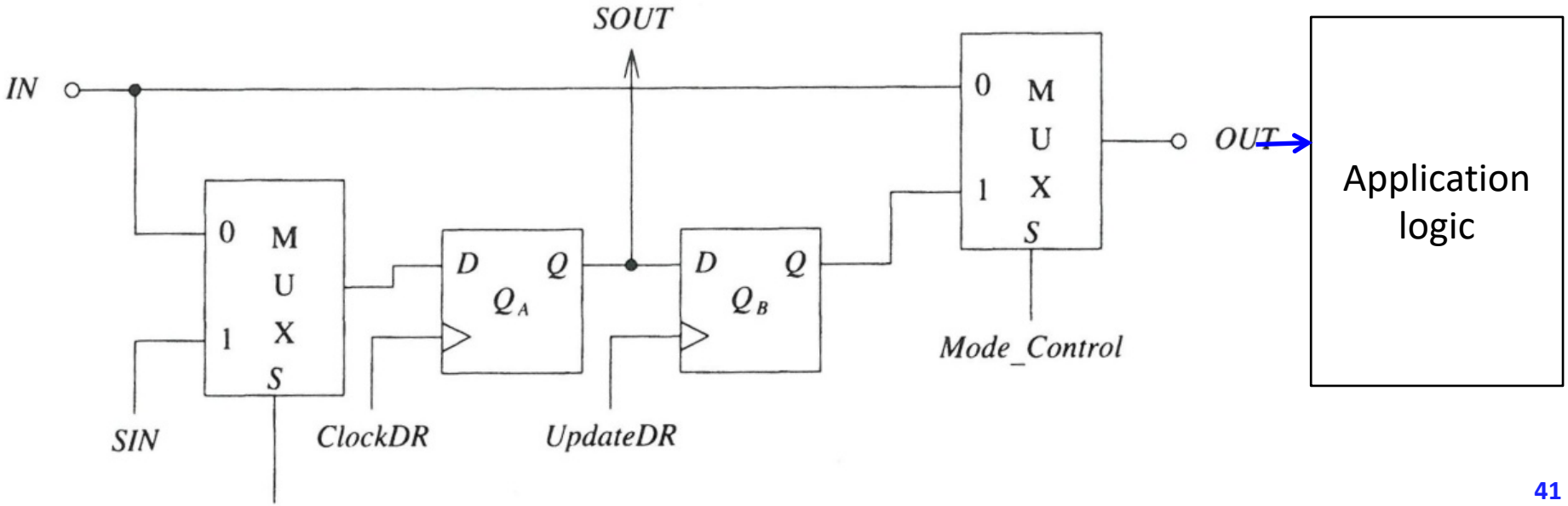


Test Bus Operation

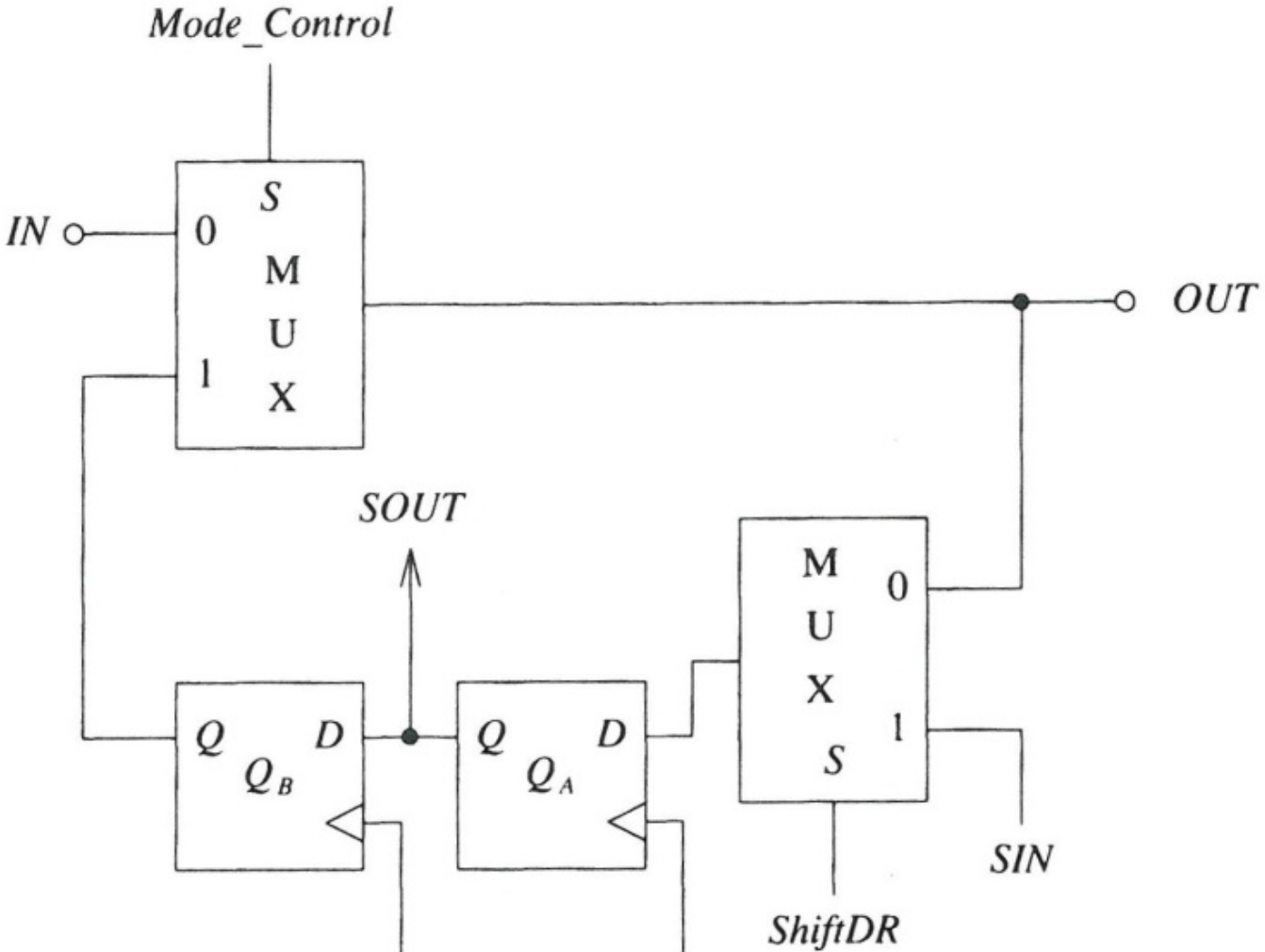
1. Instruction sent serially over the TDI line into the instruction register
2. Selected test circuitry is configured to respond to the instruction
   - More data needed to configure data registers
3. The test instruction is executed. Test results can be shifted out of selected registers and transmitted over TDO line to the bus master. Data can shifted in while results are shifted out.

Boundary Scan Cell

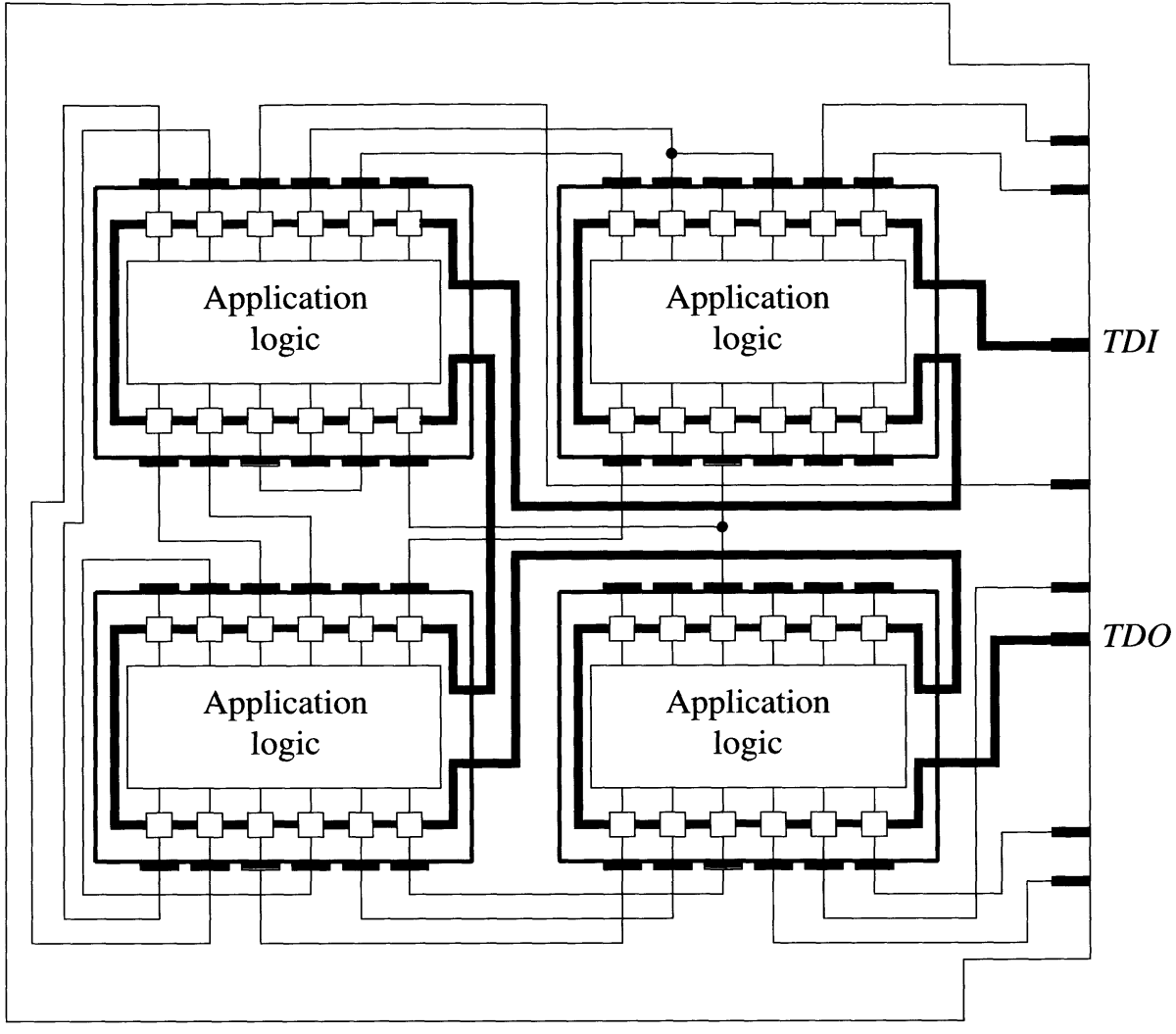
- **Normal Mode**: *Mode_Control* = 0, cell is transparent
- **Scan Mode** – Boundary cells are interconnected into a scan path (TDI input, TDO output) *ShiftDR* =1 and Clock pulses applied to *ClockDR*
- **Capture Mode** – *ShiftDR* = 0 => input IN is *captured*
- **Update Mode** – Once Q_A is loaded (by scan/capture), set *Mode_control* = 1 and apply a clock pulse to *UpdateDR* for the value in Q_A applied to OUT



Boundary Scan Cell – Another Design



PCB with IEEE 1149.1 bus

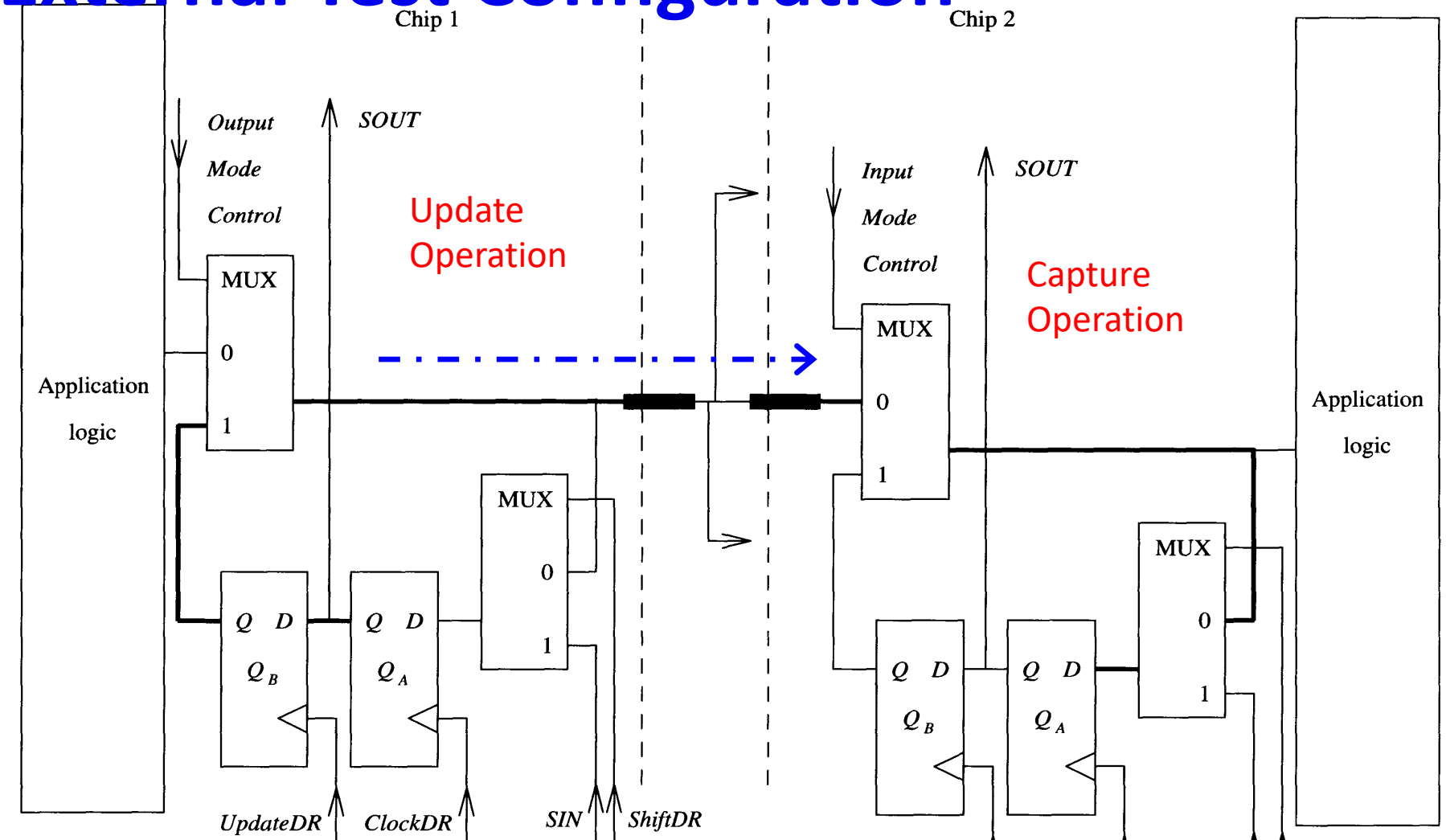


- Interconnect Test
- System Snapshot
- Chip Test

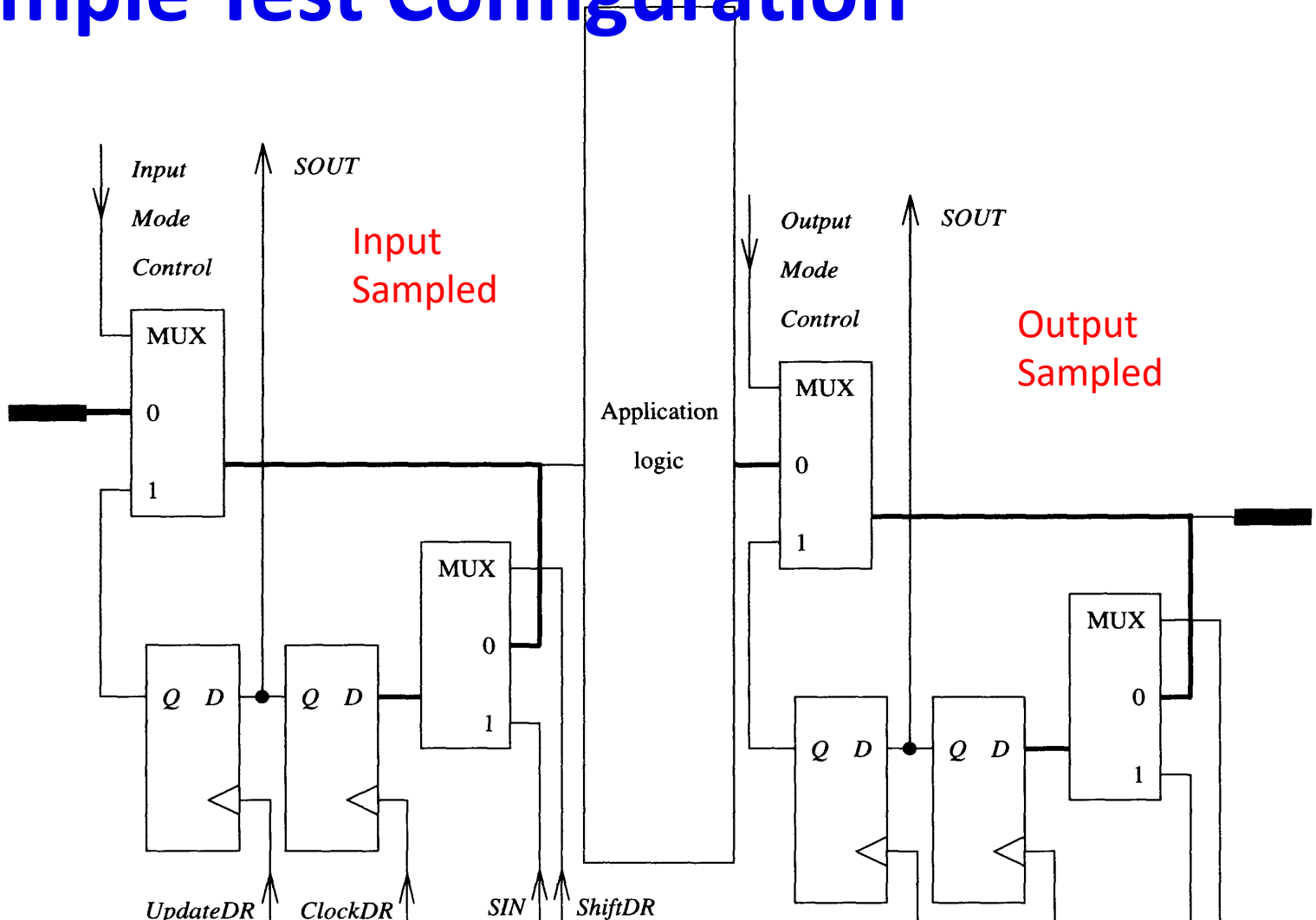
PCB Test – Three modes

- External Test Mode
  - Test interconnects between chips
- Sample Test Mode
  - I/O data of a chip can be sampled during normal system operation – snapshots of chip IO data
  - Sampled data can be scanned out while board is in normal operation
- Internal Test Mode
  - Inputs to the application logic is driven by the input boundary-scan cells and response captured in output boundary-scan cells

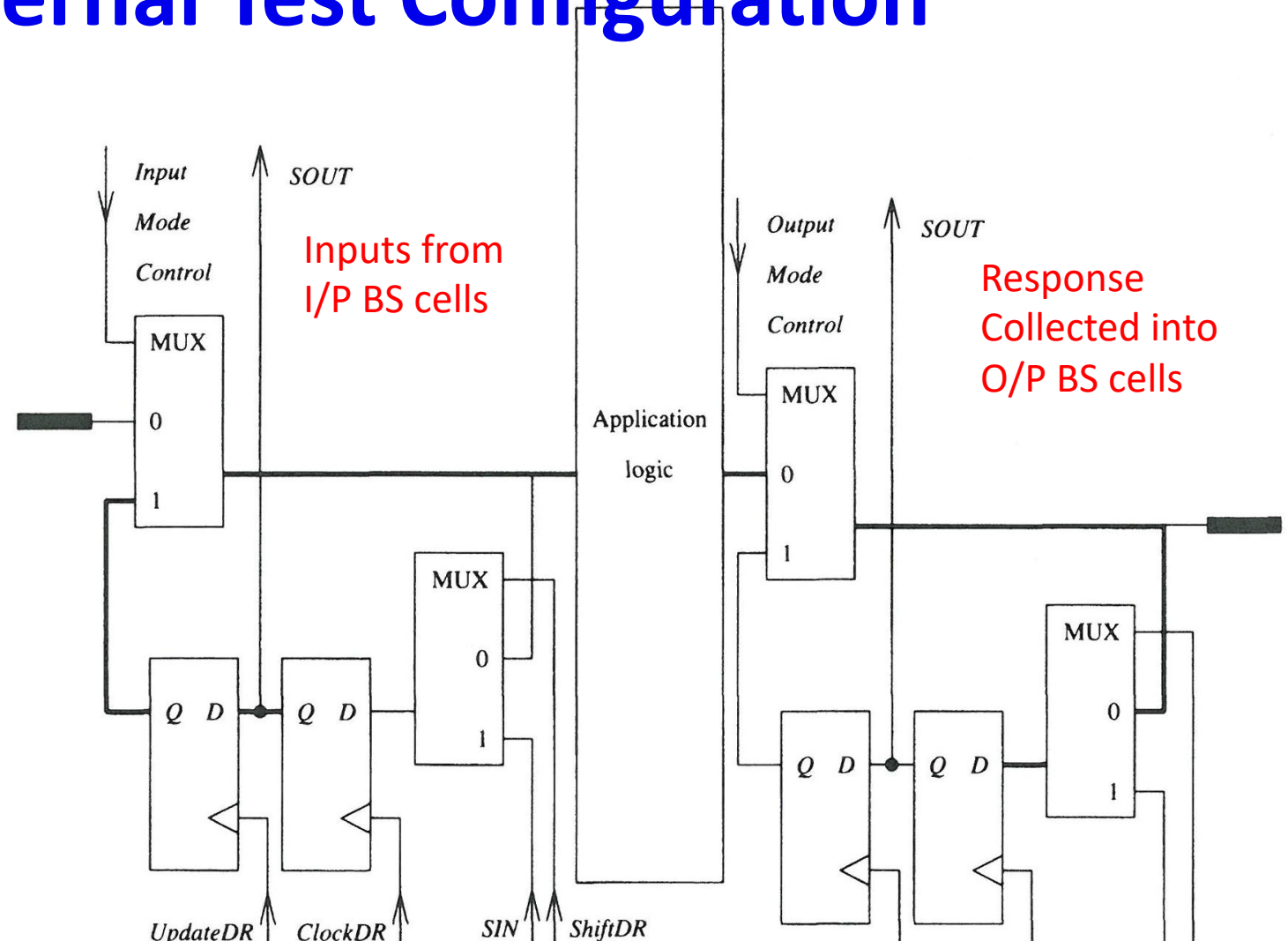
External Test Configuration

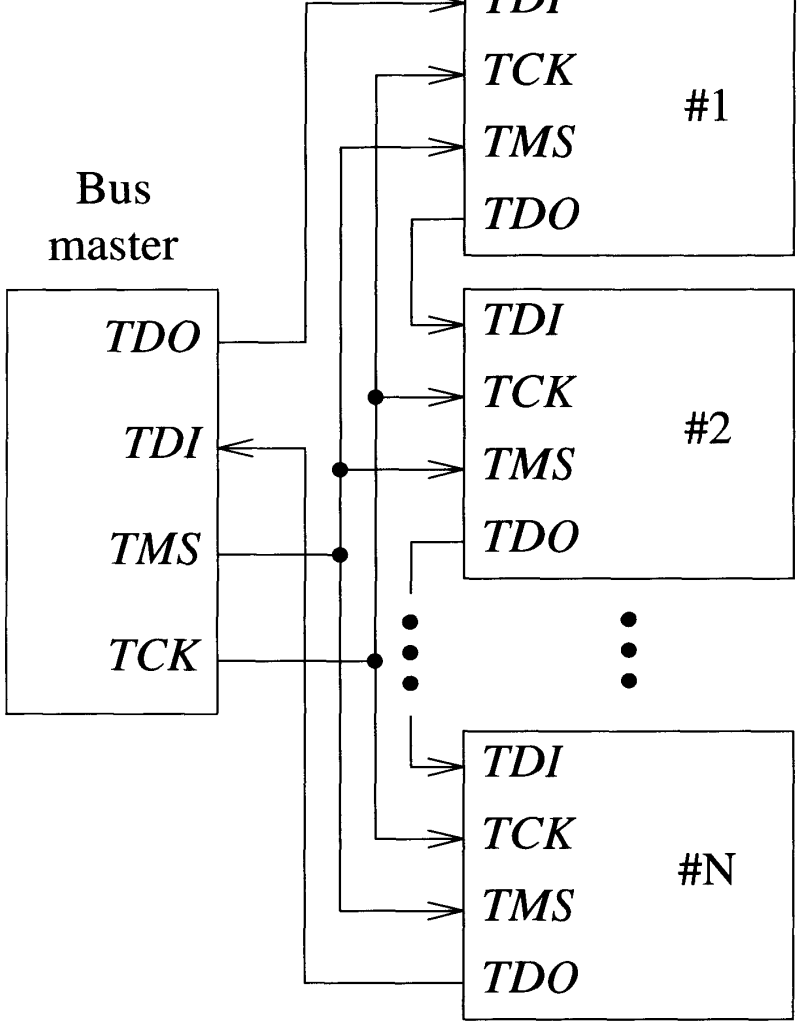


Sample Test Configuration

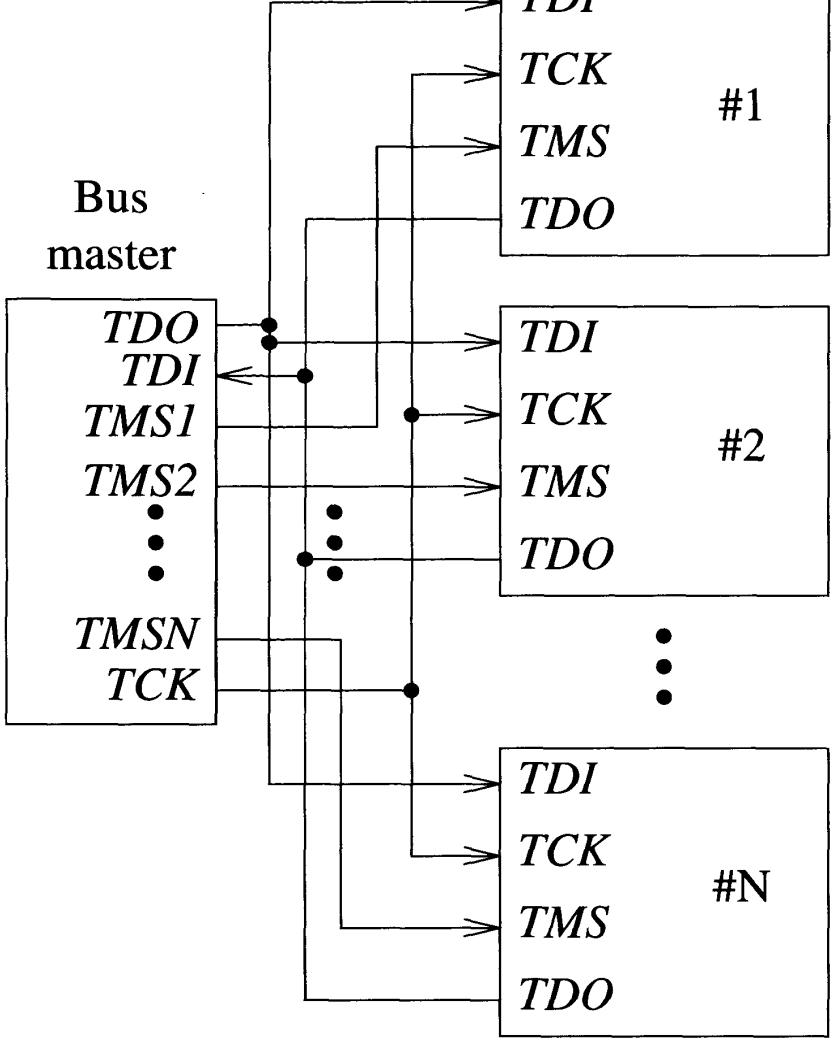


Internal Test Configuration




Bus
master
TDO
TDI
TMS
TCK
TDI
TCK
TMS
TDO
#1
TDI
TCK
TMS
TDO
#2
TDI
TCK
TMS
TDO
#N

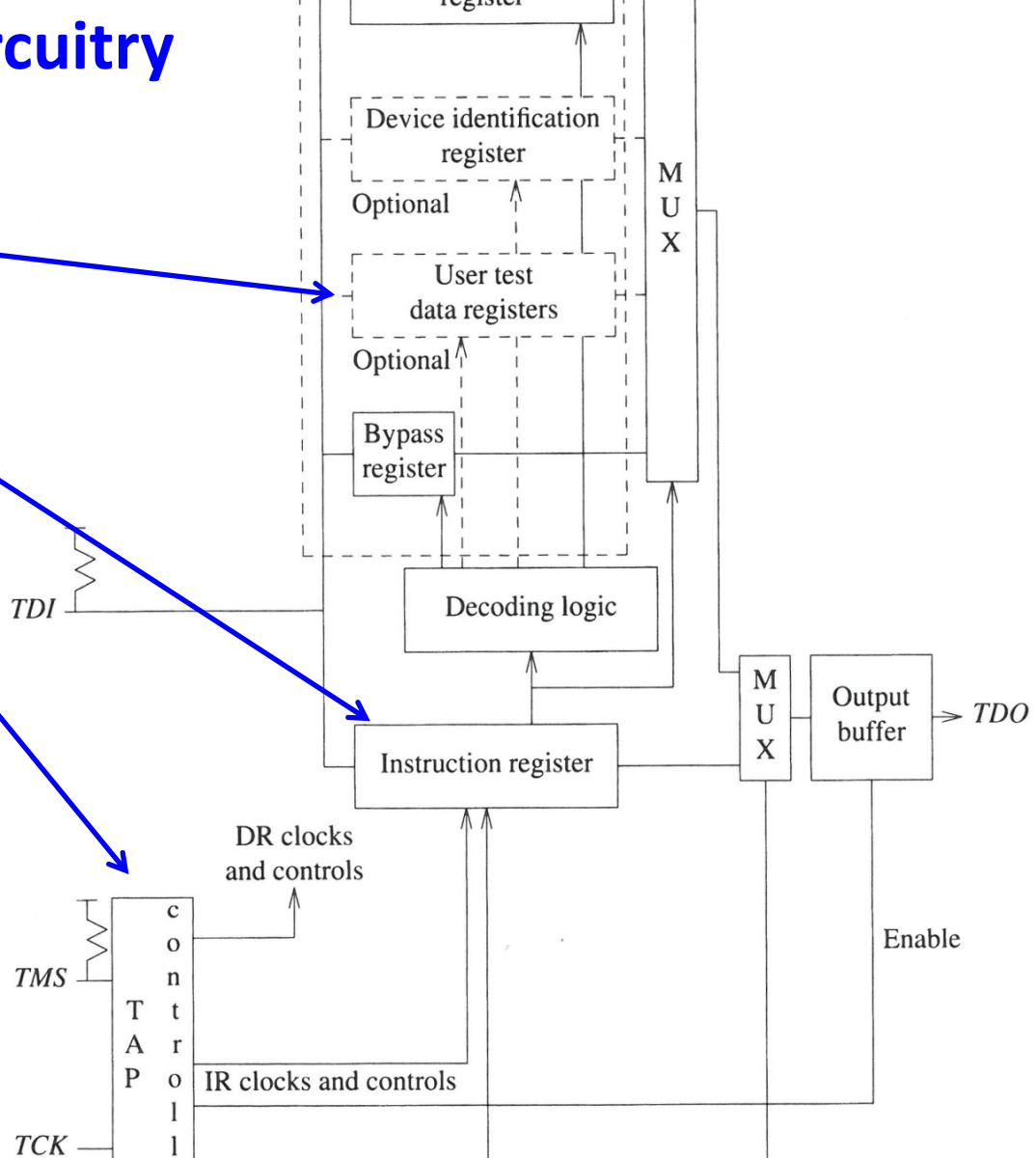
(a)


Bus
master
TDO
TDI
TMS1
TMS2
TMSN
TCK
TDI
TCK
TMS
TDO
#1
TDI
TCK
TMS
TDO
#2
TDI
TCK
TMS
TDO
#N

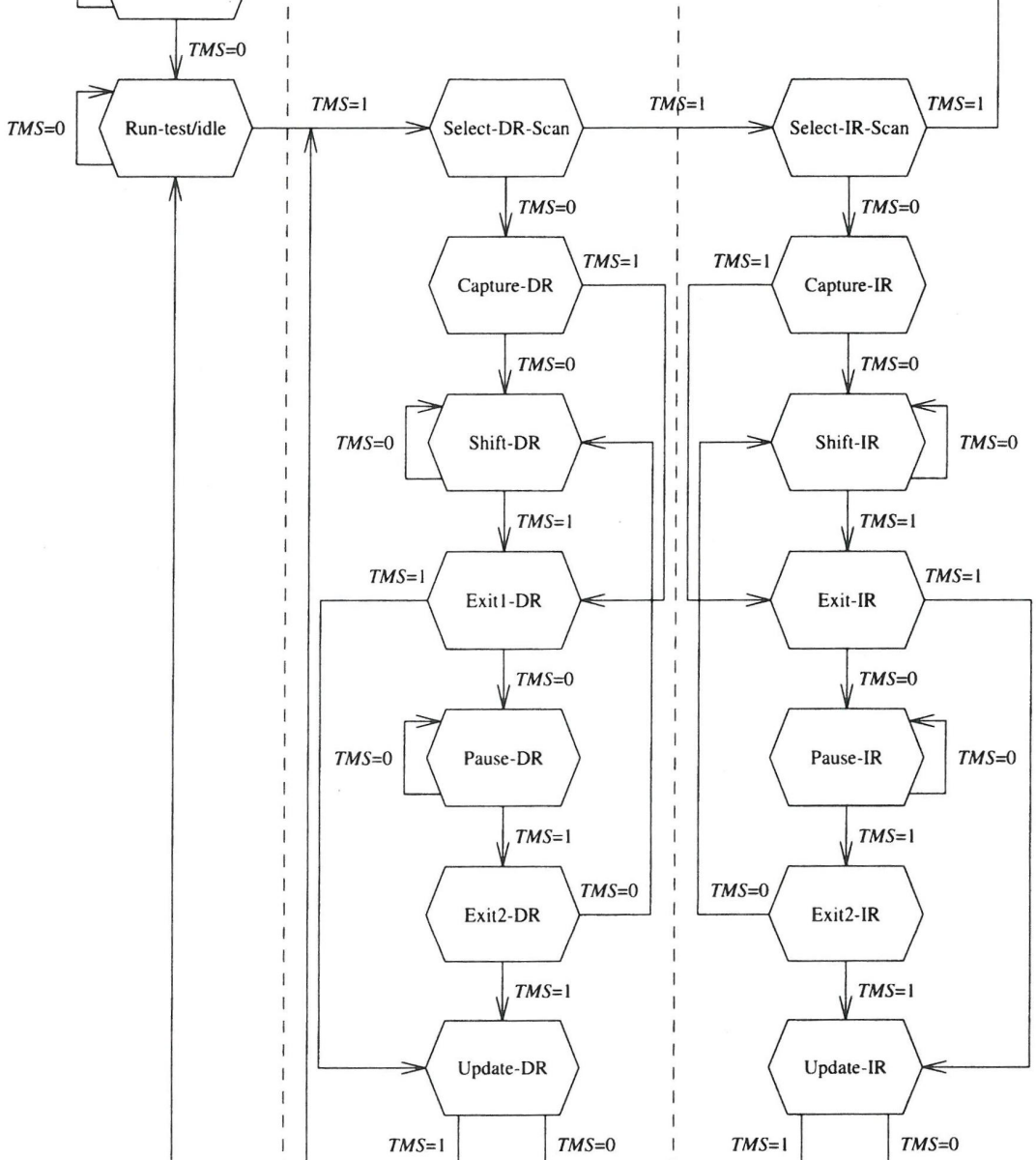
(b)

IEEE 1149.1 Test Bus Circuitry

- TAP – TCK, TMS, TDI, TDO
- Test DR
- Scannable IR
- TAP controller



State Diagram of TAP Controller



Instruction Register and Commands

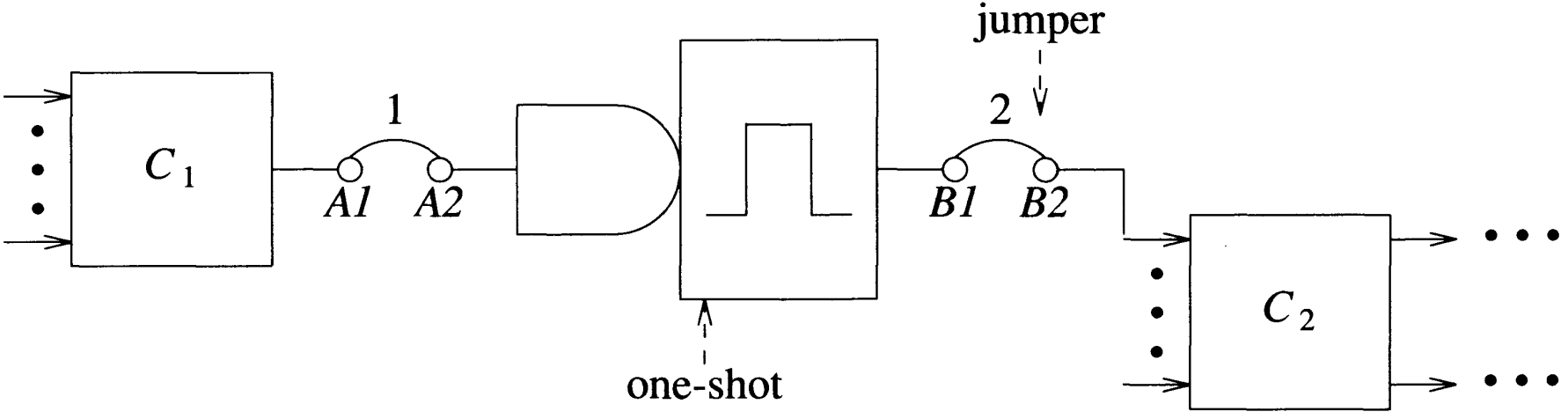
- Commands can be shifted into IR from TDI.
- Commands specify operations and selection of DR.
  - **BYPASS** – exclude a chip from scan path.
  - **EXTEST** – test intra-chip interconnect
  - **SAMPLE** – capture chip IO and store data on boundary scan registers.
  - **INTEST** – test a chip itself.
  - **RUNBIST** – support a self-testing.

Backup

3 – Monostable Multivibrators

Rule: *Disable internal one-shots during test*

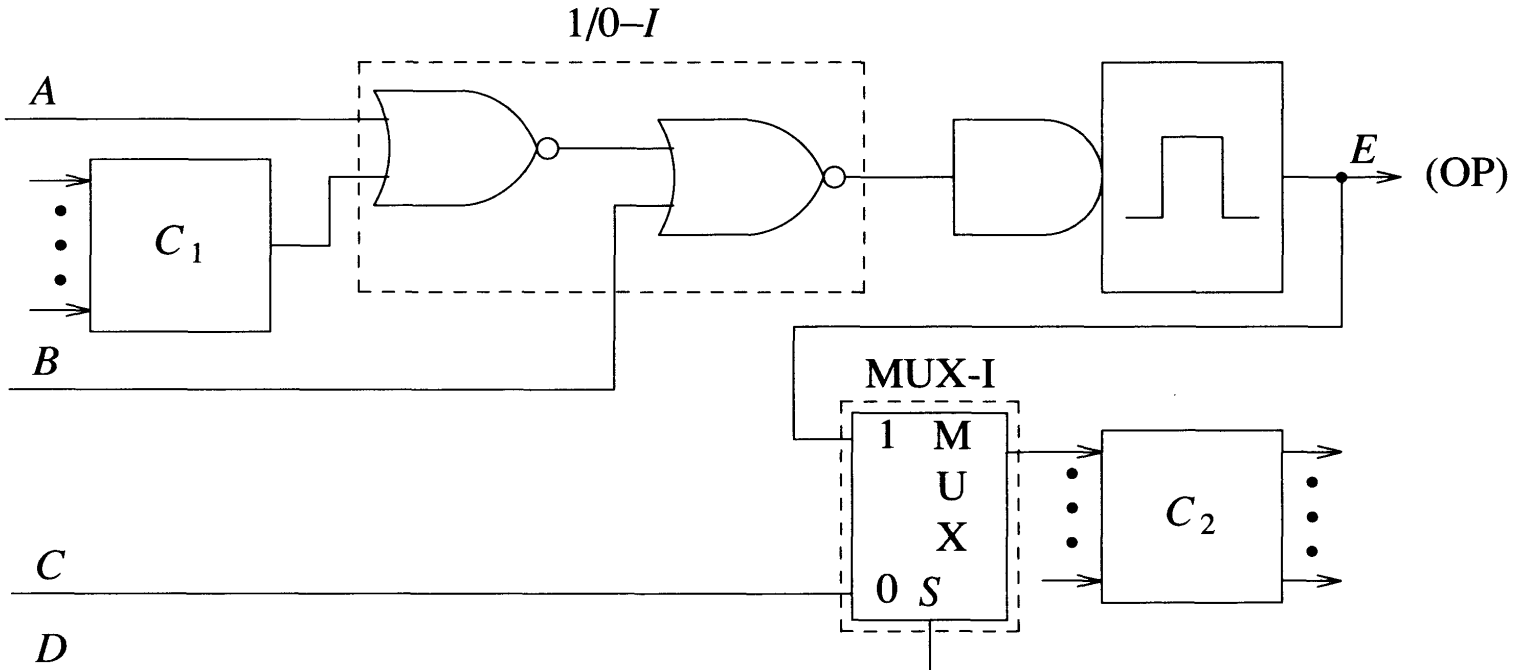
- One-shots provide pulses internal to circuit
- Difficult for ATE to remain in synchronization with the circuit



3 – Monostable Multivibrators

Rule: *Disable internal one-shots during test*

- One-shots provide pulses internal to circuit
- Difficult for ATE to remain in synchronization with the circuit



4 – Oscillators and Clocks

Rule: *Disable internal oscillators/clocks during test*

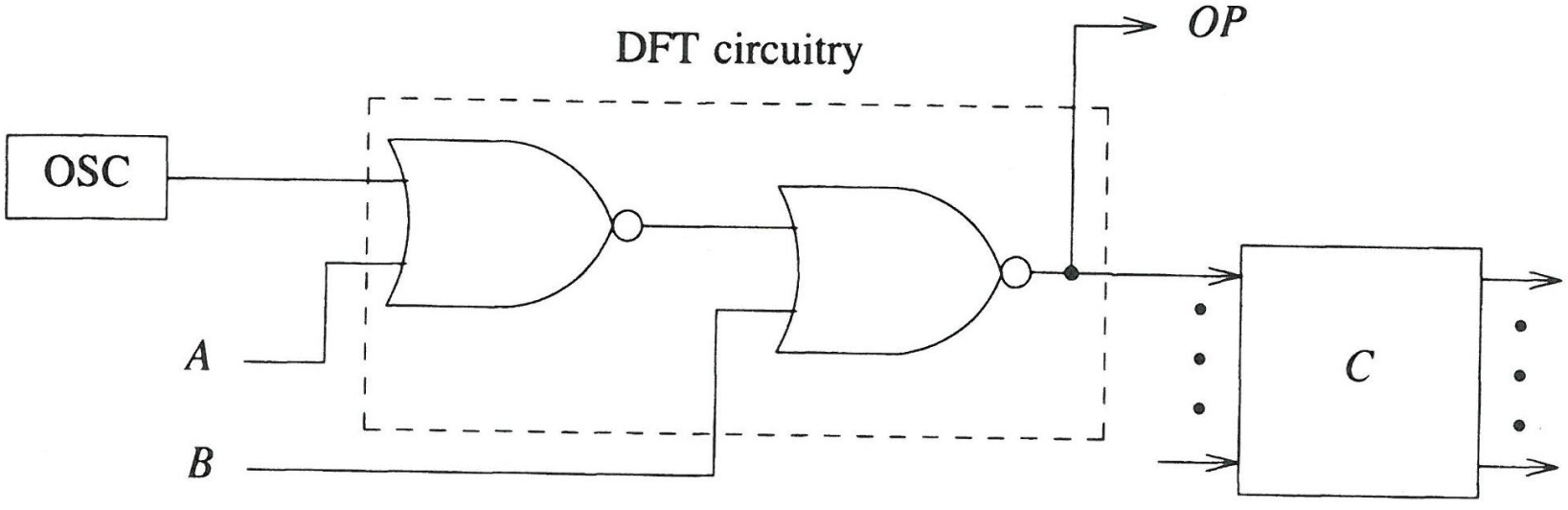


Figure 9.9 Testability logic for an oscillator