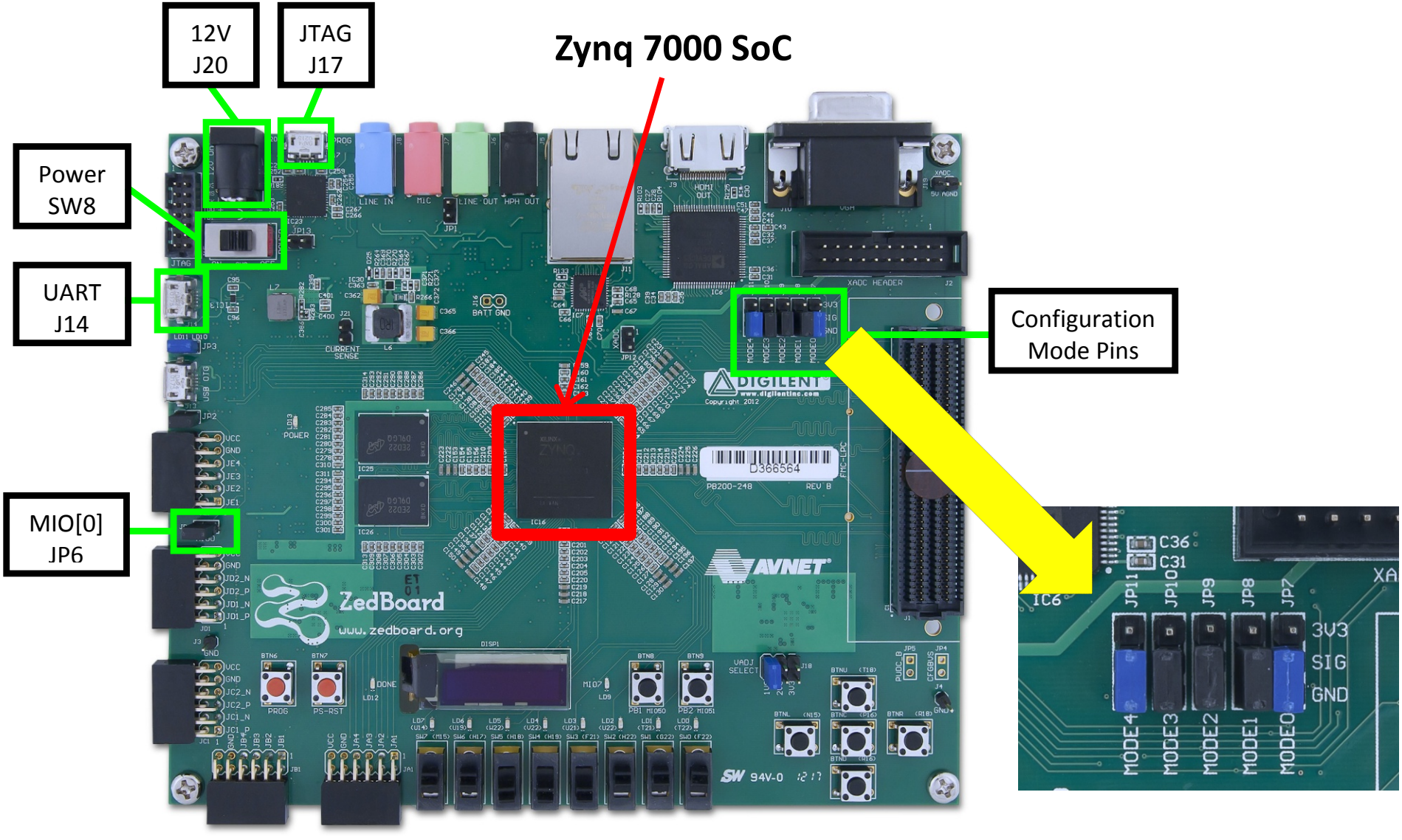
CDA 4253 FPGA System Design
Introduction to Zynq

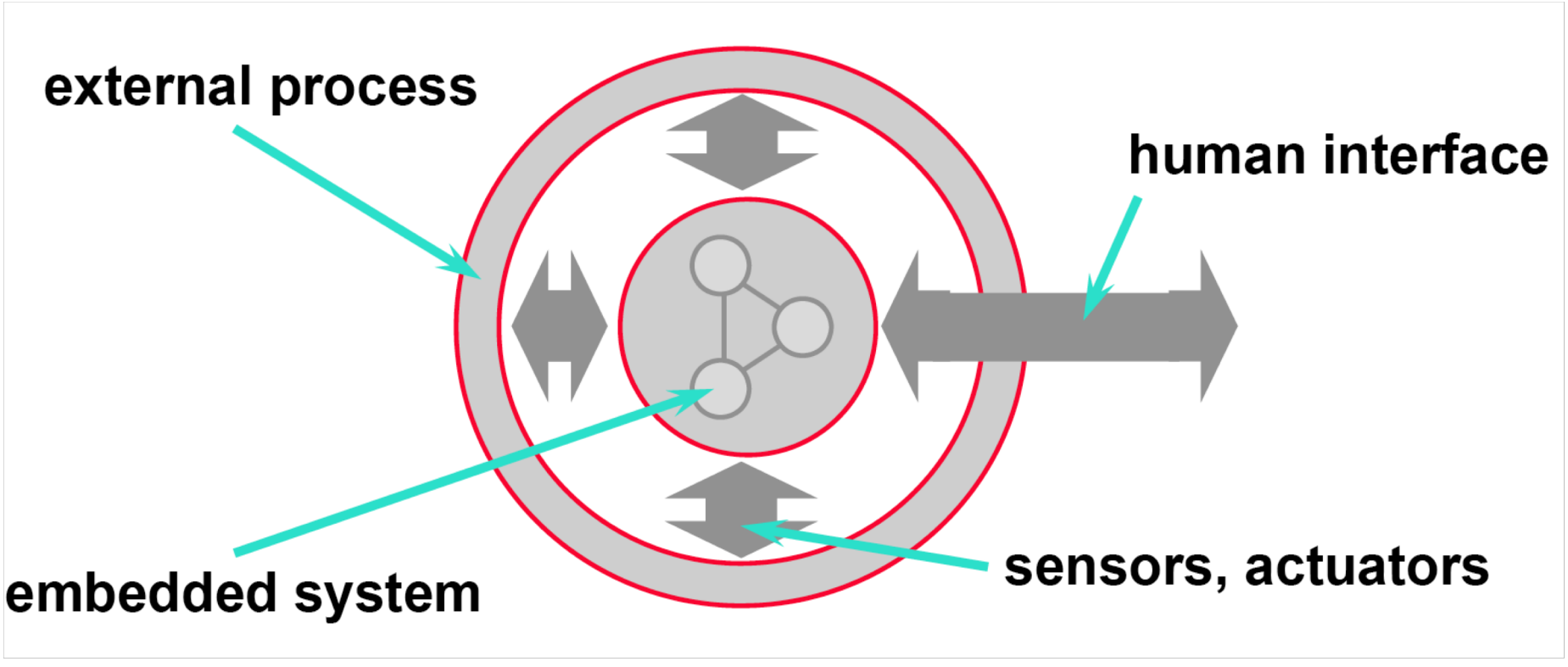
Hao Zheng
Dept of Comp Sci & Eng
U of South Florida


12V
J20
JTAG
J17
Zynq 7000 SoC
Power
SW8
UART
J14
MIO[0]
JP6
Configuration
Mode Pins
ZedBoard
www.zedboard.org
AVNET
DIGILENT
MODE4
MODE3
MODE2
MODE1
MODE0
3V3
SIG
GND

Key Features

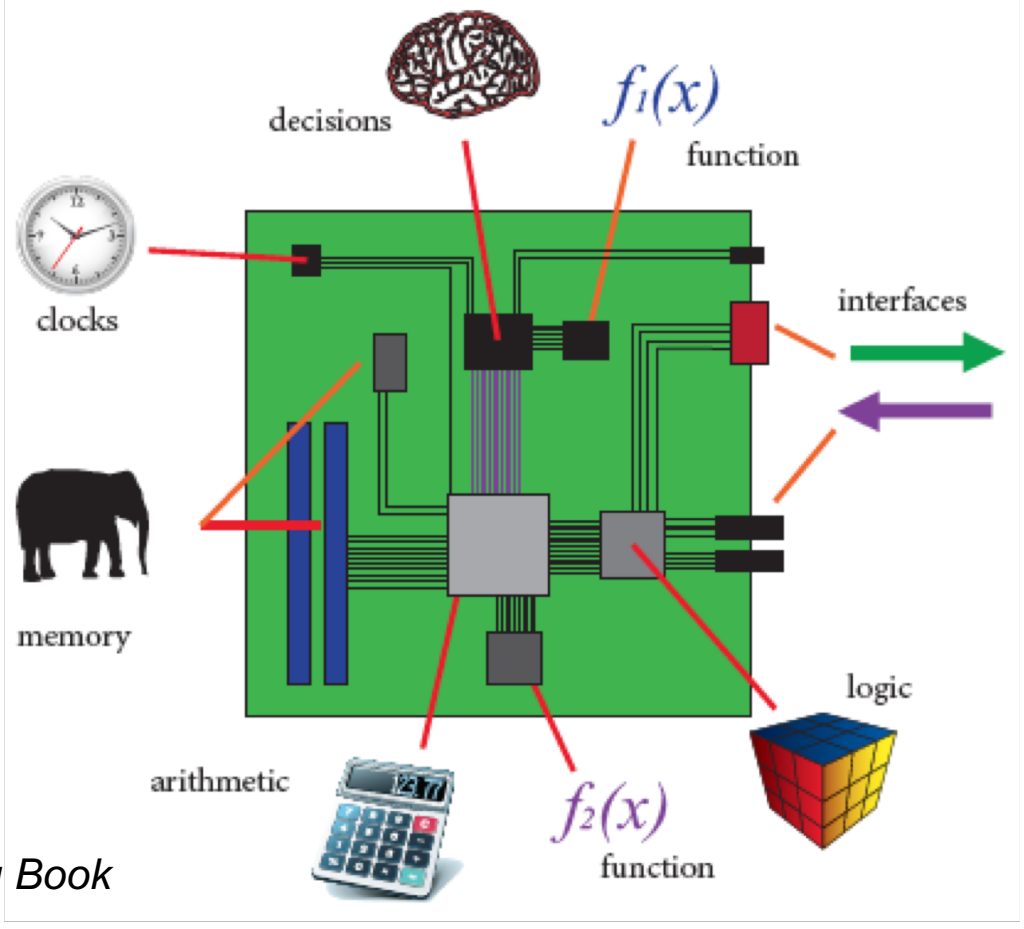
- Processor – Zynq-7000 AP SoC
- Memory
  - 512 MB DDR3
  - 256 Mb Quad-SPI Flash
  - 4GB SDcard
- Communication
  - Onboard USB-JTAG Programming
  - 10/100/1000 Ethernet
  - USB OTG 2.0 and USB-UART
- Expansion Ports – Pmods

A General View of Embedded Systems



Source: ETHZ, Prof. Lothar Thiele

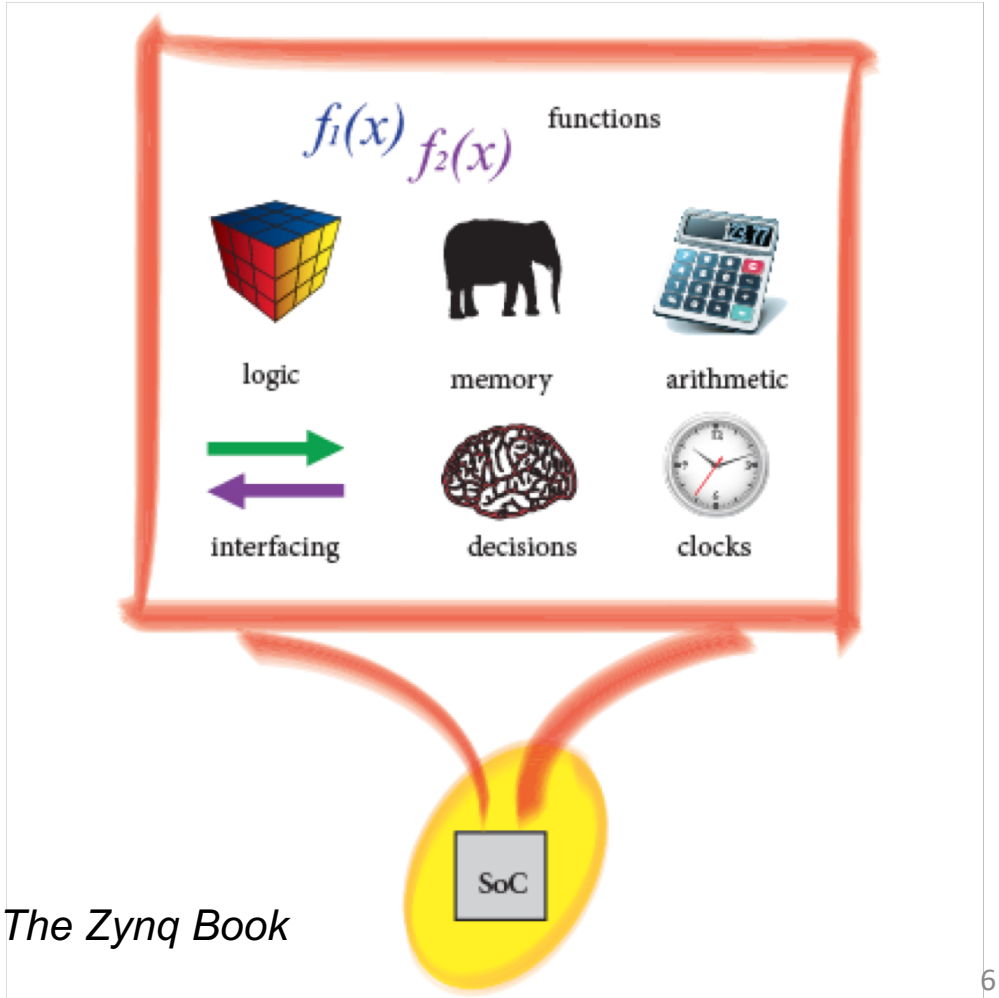
System-on-a-Board



Source: The Zynq Book

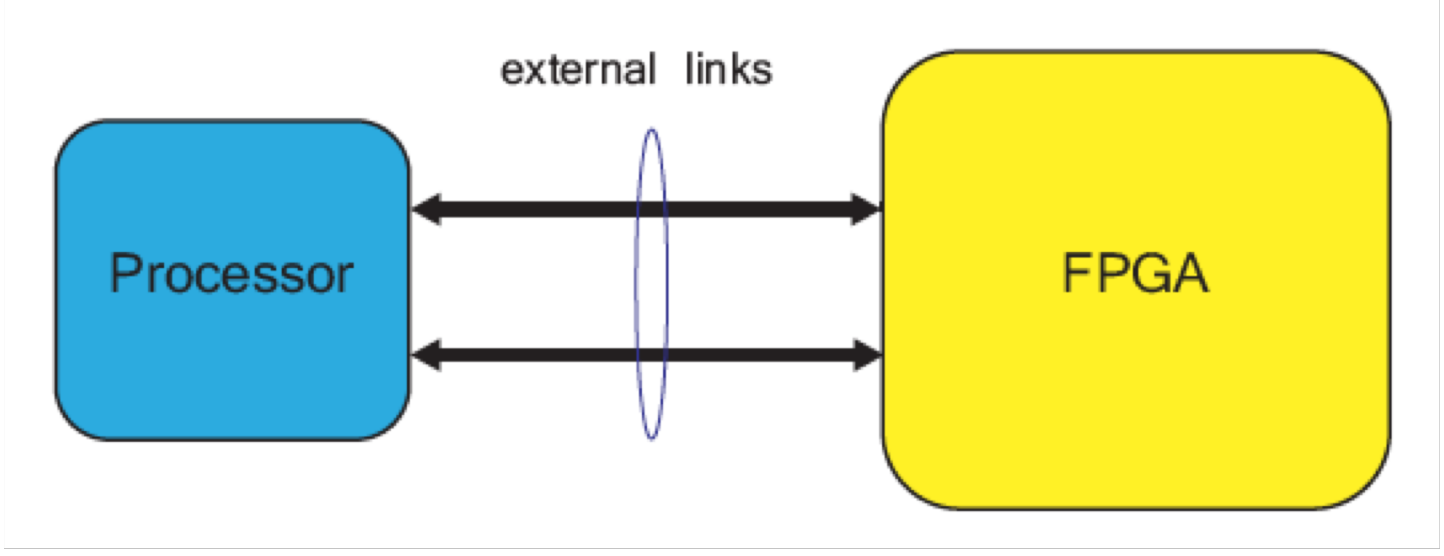
System-on-a-Chip (SoC)

- Higher performance
- Lower power use
- Small form factor
- Reduced cost
- flexibility



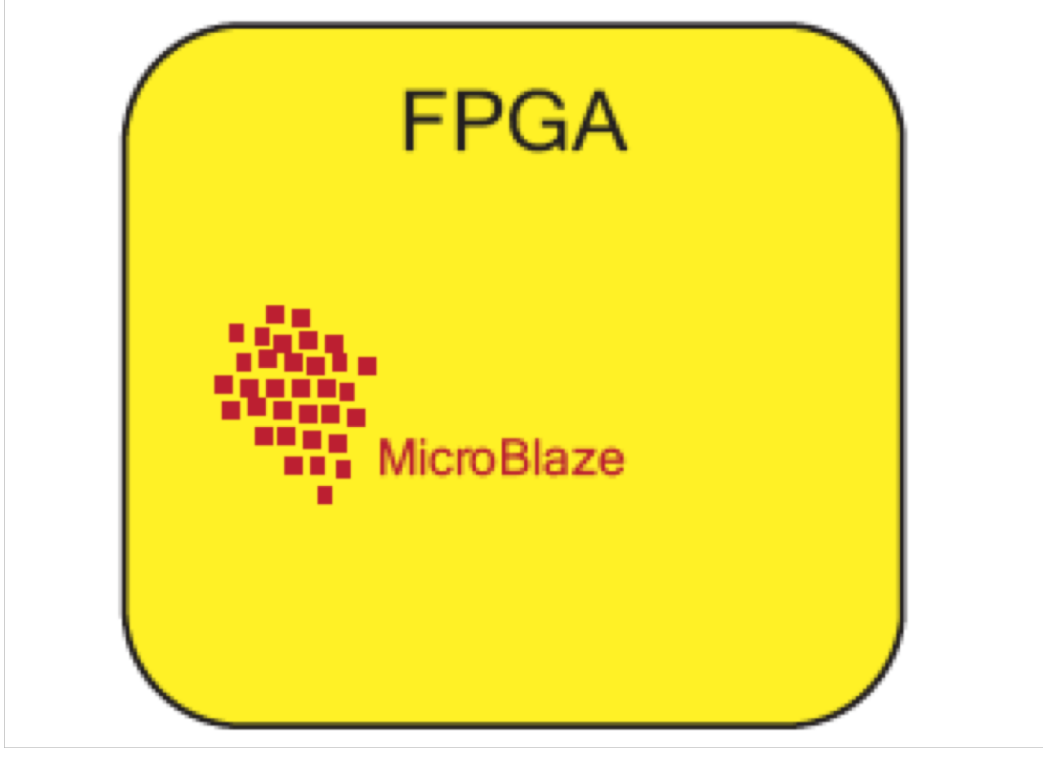
Source: The Zynq Book

How Are FPGAs used in the Past?



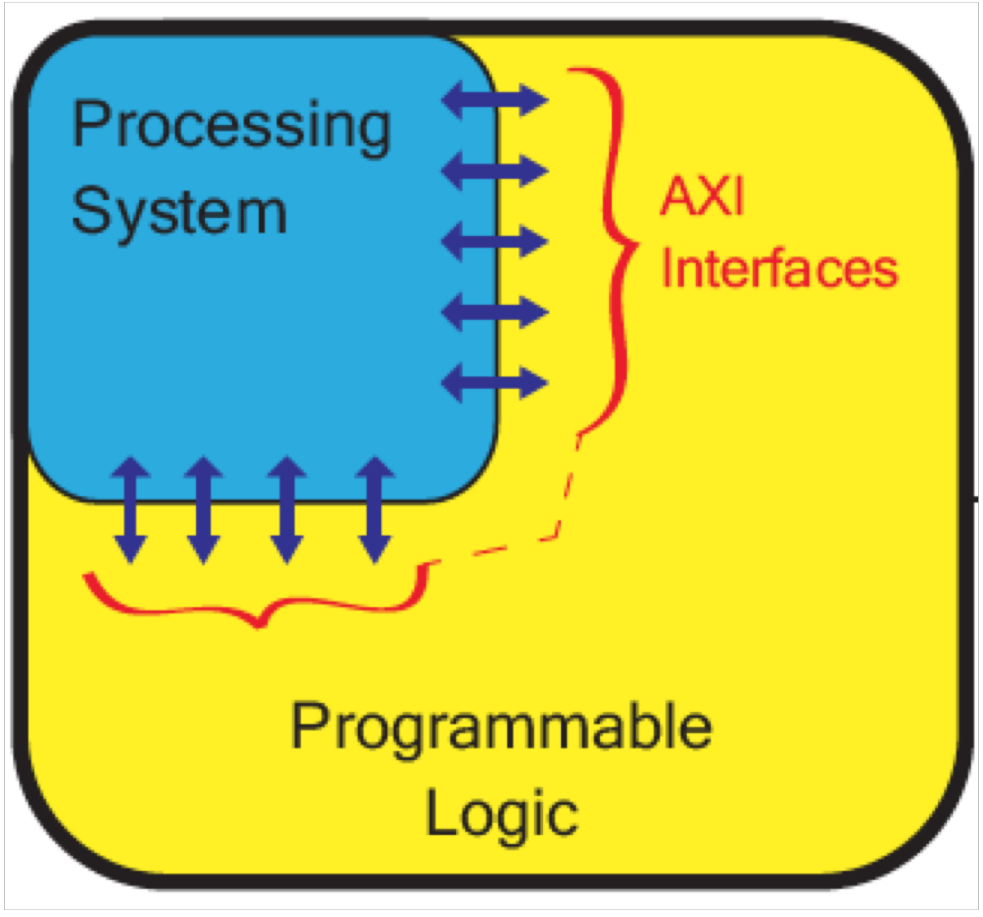
Source: The Zynq Book

How Are FPGAs used in the Past?



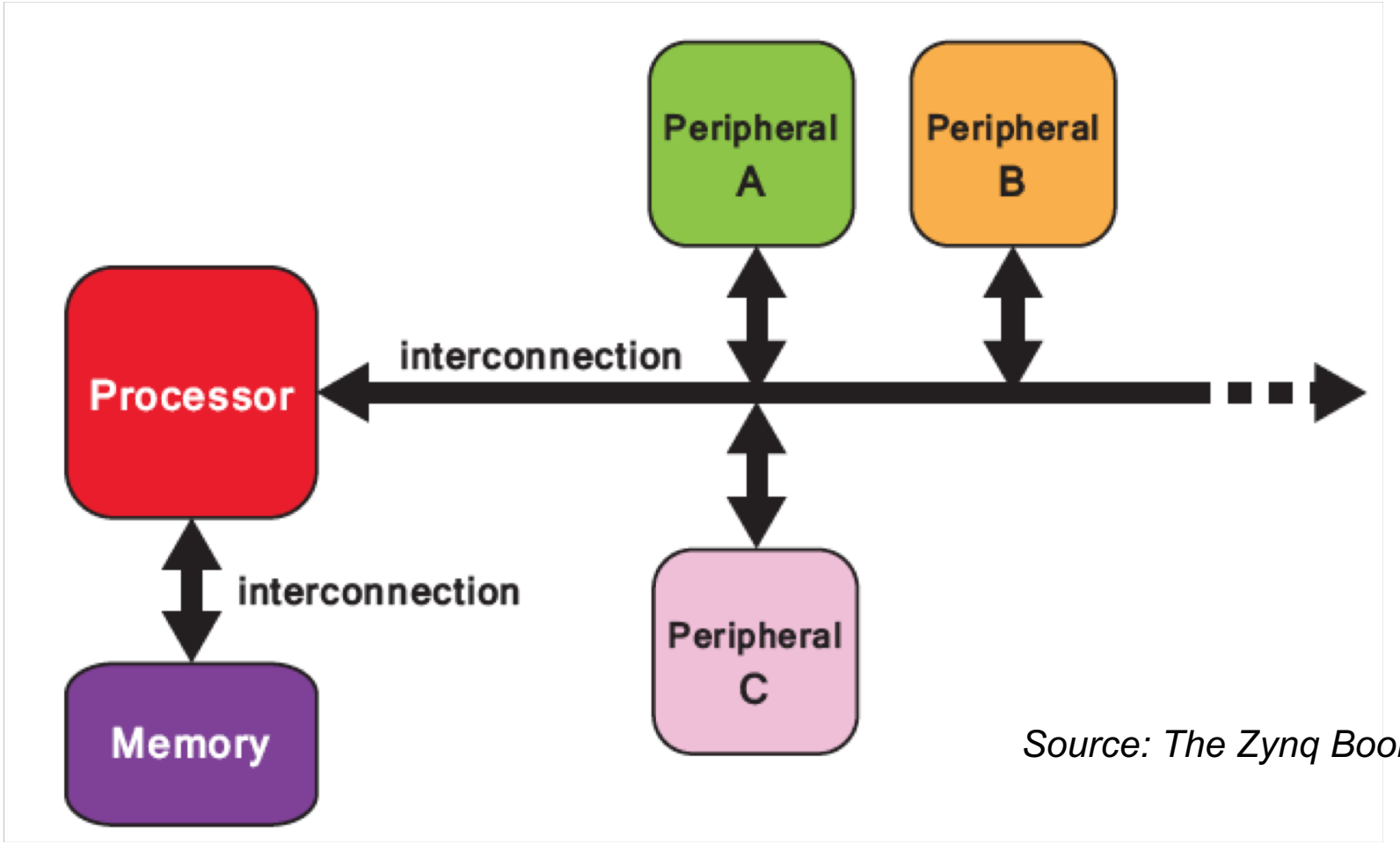
Source: The Zynq Book

Zynq – All Programmable SoC



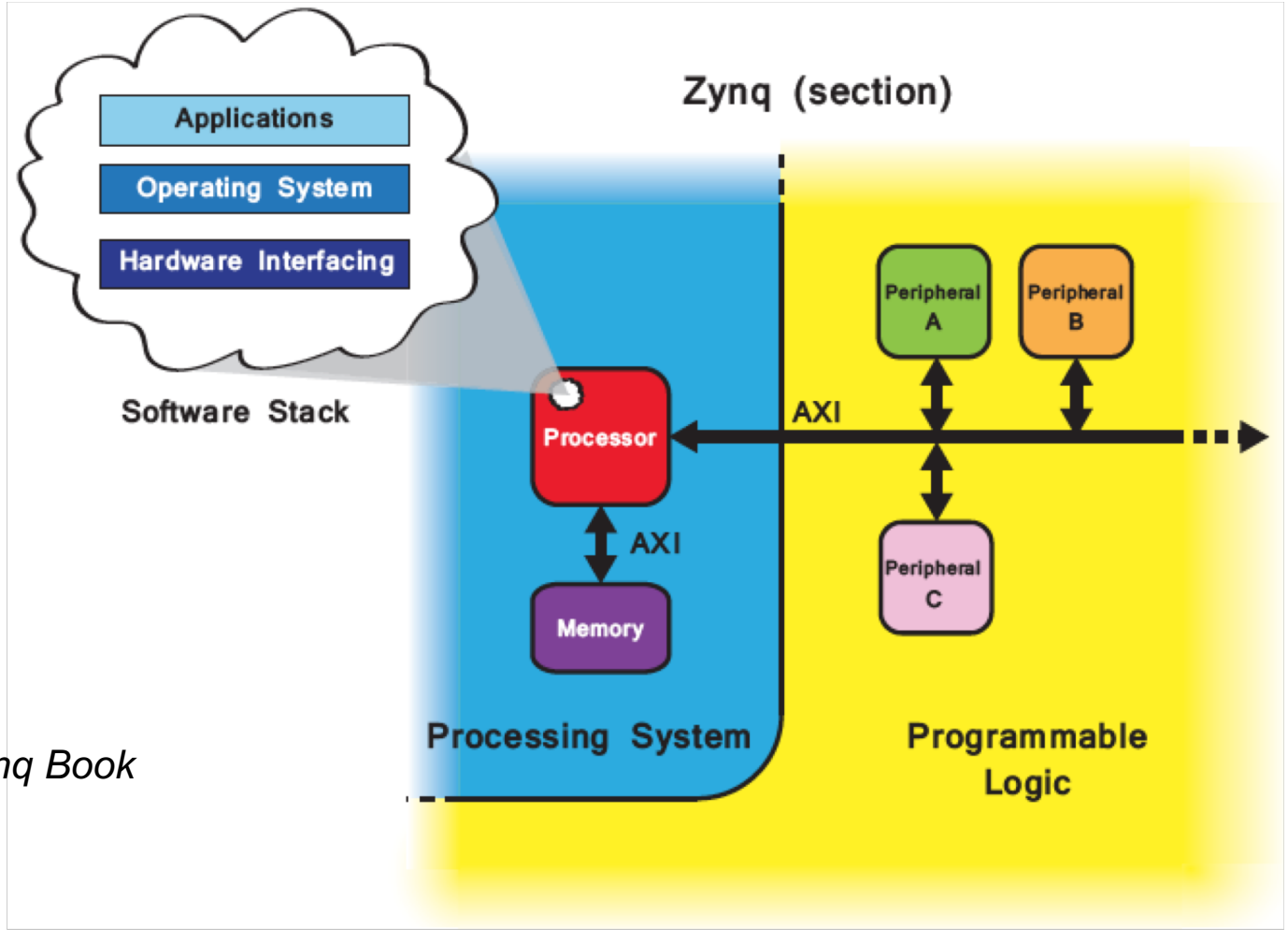
Source: The Zynq Book

Generic Embedded Architecture



Source: The Zynq Book

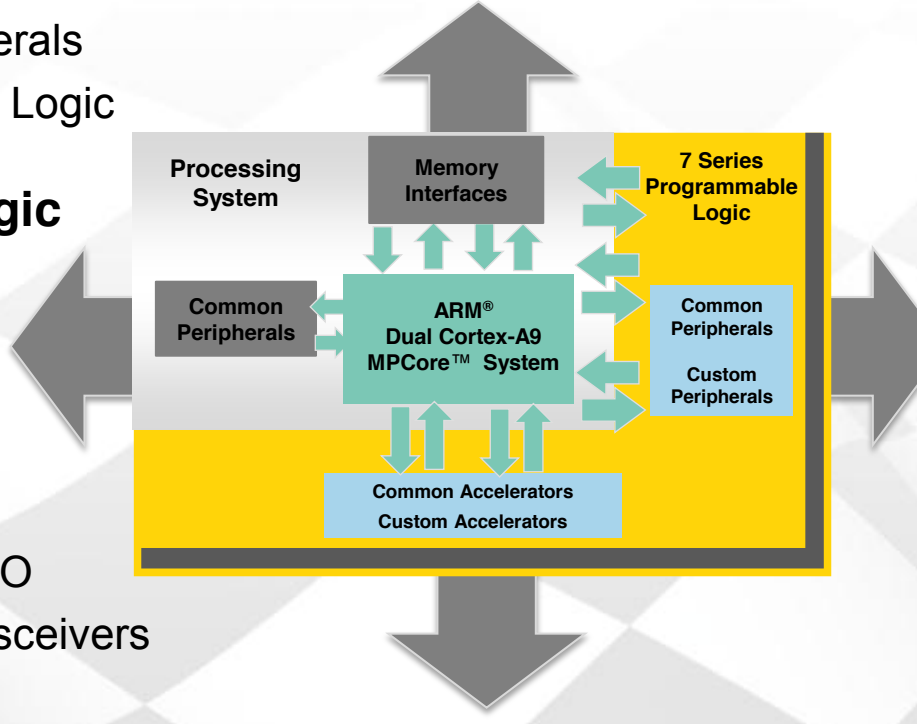
Generic Embedded Architecture – Mapping to Zynq



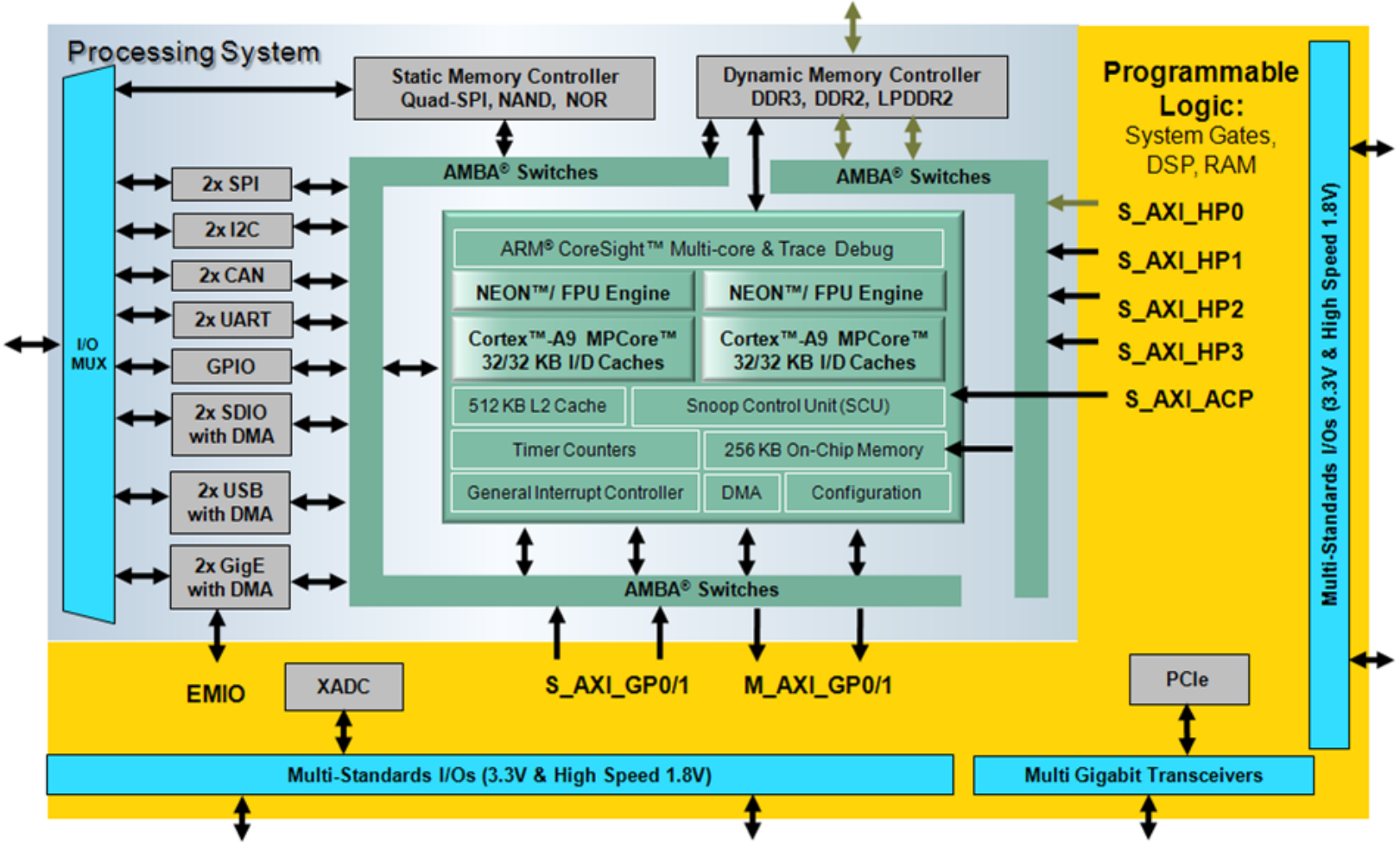
Source: The Zynq Book

Zynq 7000 SoC

- **Complete ARM®-based Processing System**
  - Dual ARM Cortex™-A9 MPCore™, processor centric
  - Integrated memory controllers & peripherals
  - Fully autonomous to the Programmable Logic
- **Tightly Integrated Programmable Logic**
  - Used to extend Processing System
  - Scalable density and performance
  - Over 3000 internal interconnects
- **Flexible Array of I/O**
  - Wide range of external multi-standard I/O
  - High performance integrated serial transceivers
  - Analog-to-Digital Converter inputs



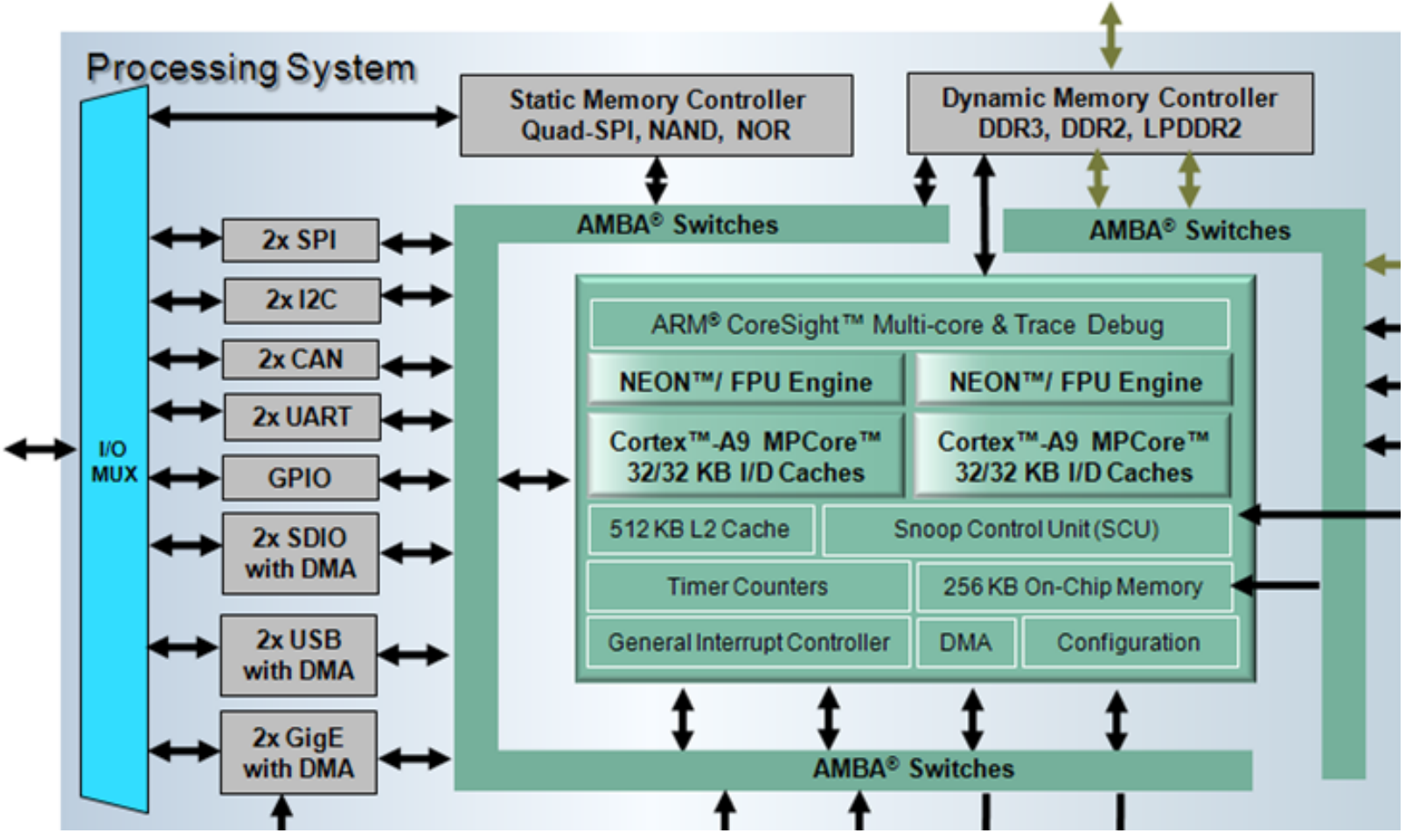
Zynq-7000 SoC Block Diagram



PS and PL

- PS: Processing system, hard silicon core
  - Dual ARM Cortex-A9 processor based
  - Multiple peripherals
- PL: Programmable logic
  - Shares the same 7 series programmable logic as
    - Artix-based devices: Z-7010 and **Z-7020** (high-range I/O banks only)
    - Kintex-based devices: Z-7030 and Z-7045 (mix of high-range and high-performance I/O banks)

PS Components

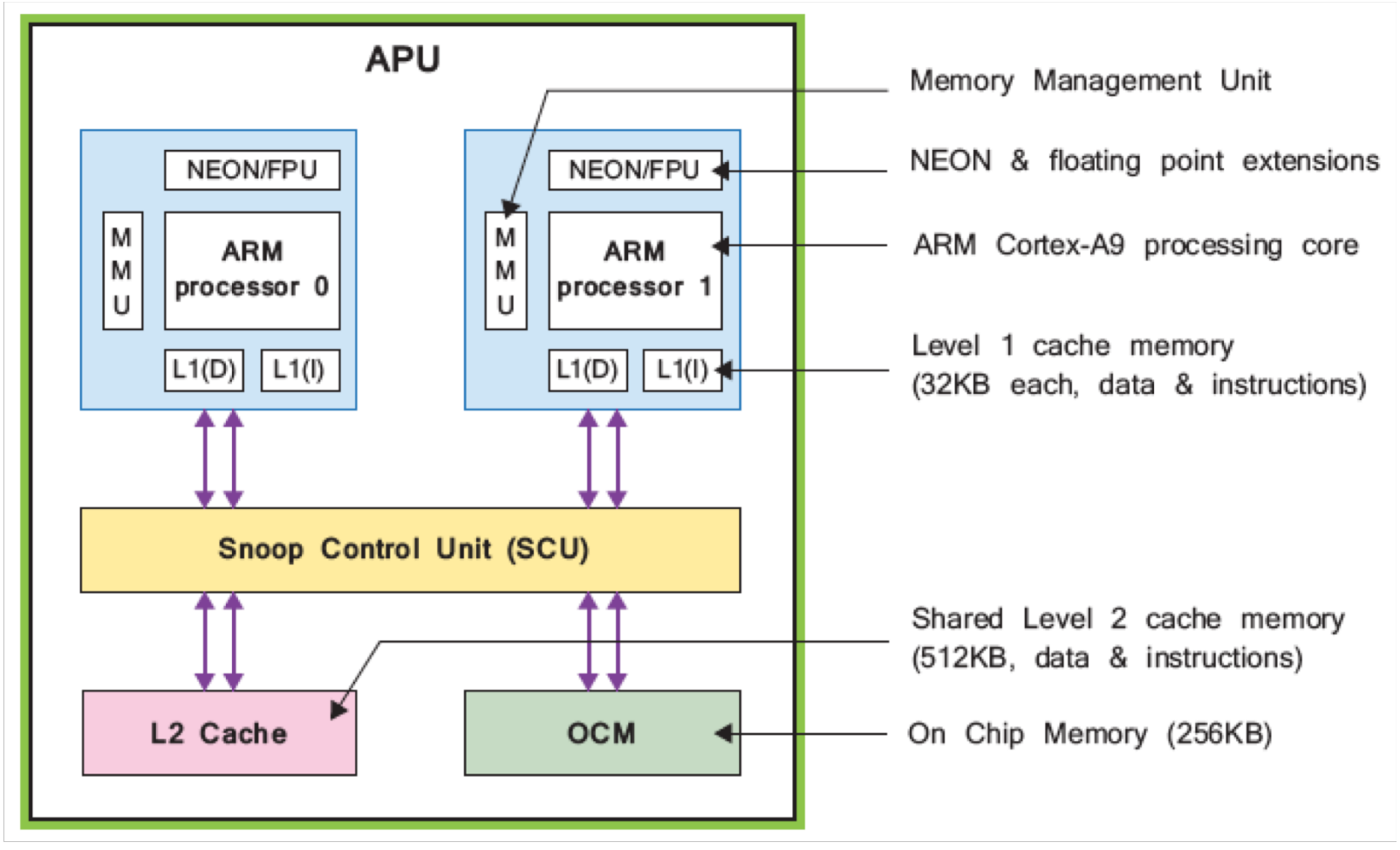


PS Components

- Application processing unit (APU)
- I/O peripherals
  - Multiplexed I/O (MIO),
  - extended multiplexed I/O (EMIO)
- Memory interfaces
- PS interconnect
- DMA
- Timers
- General interrupt controller (GIC)
- On-chip memory (OCM)
- Debug controller: ARM CoreSight

Block Diagram – APU

Source: The Zynq Book

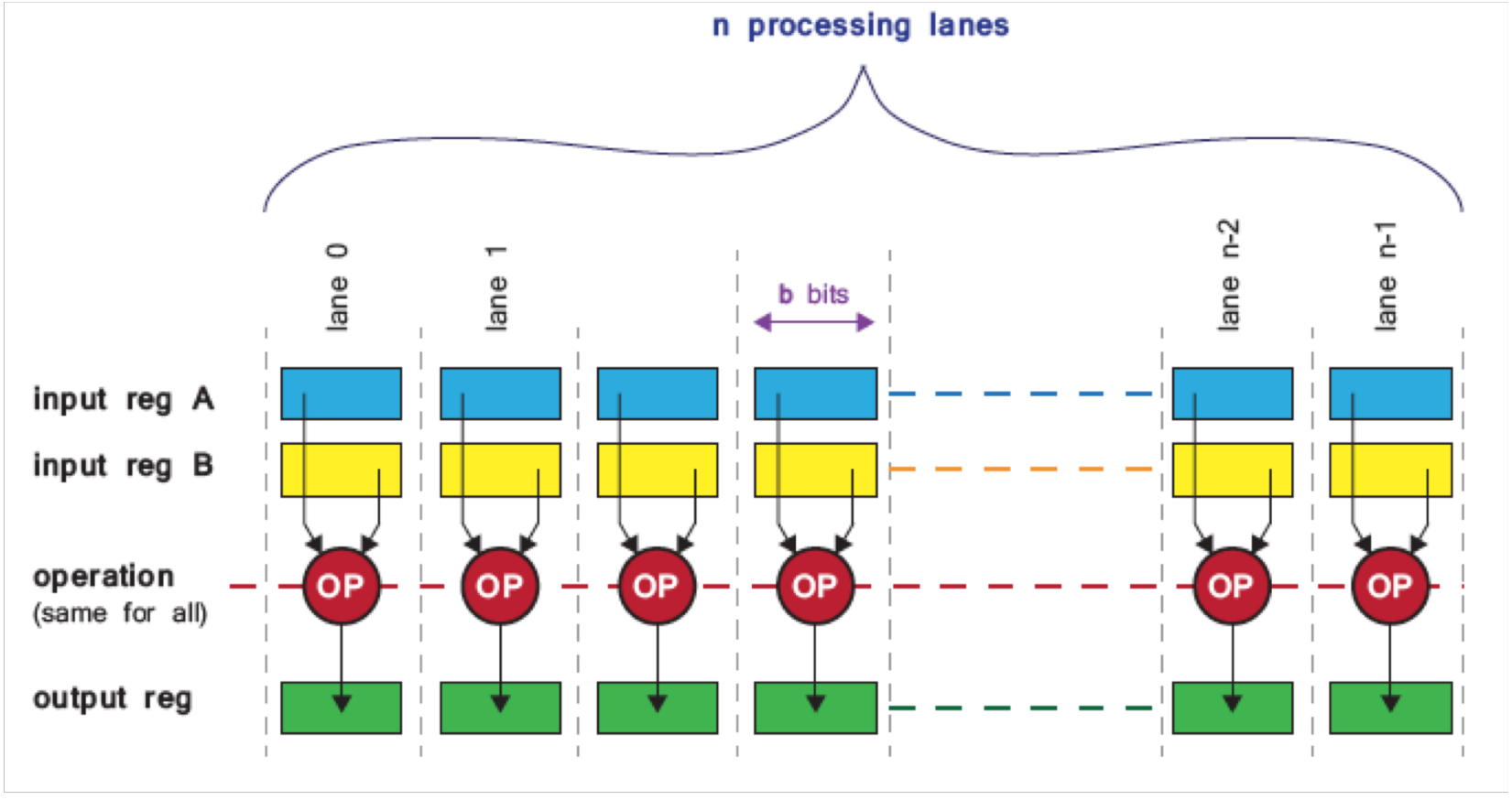


ARM Cortex–A9 Processor

- Dual-core processor cluster
- 2.5 DMIP/MHz per processor
- Harvard architecture
  - Self-contained 32KB L1 caches for instructions and data
- External memory based 512KB L2 cache
- Automatic cache coherency between processor cores
- Up to 1 GHz operation (fastest speed grade)

Architecture – NEON

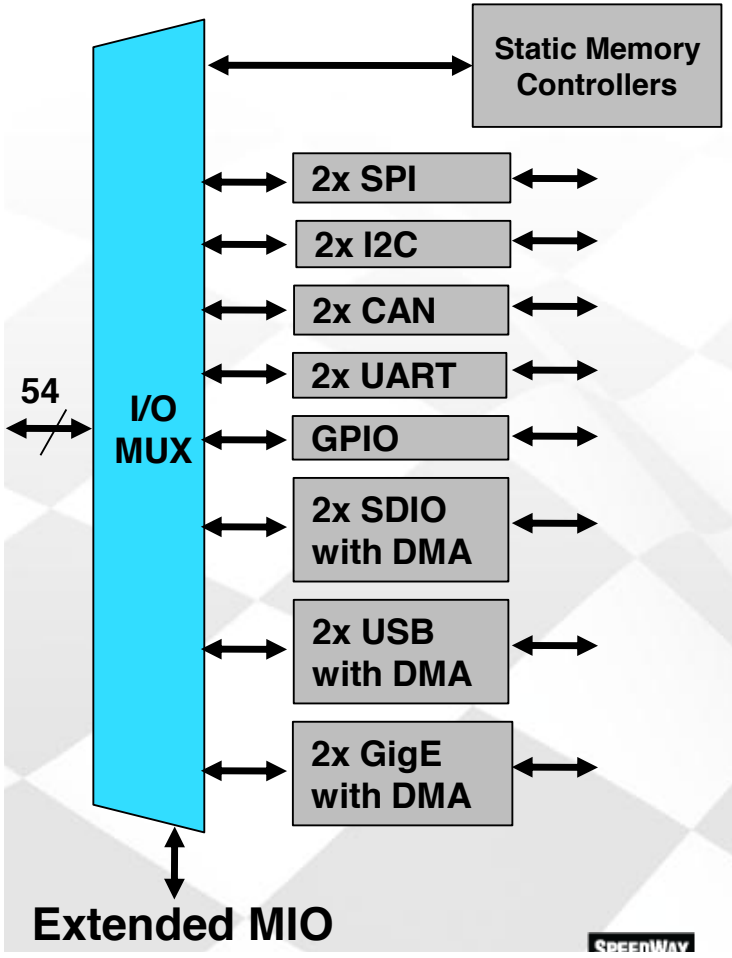
Source: The Zynq Book



For image and video processing

PS Peripherals

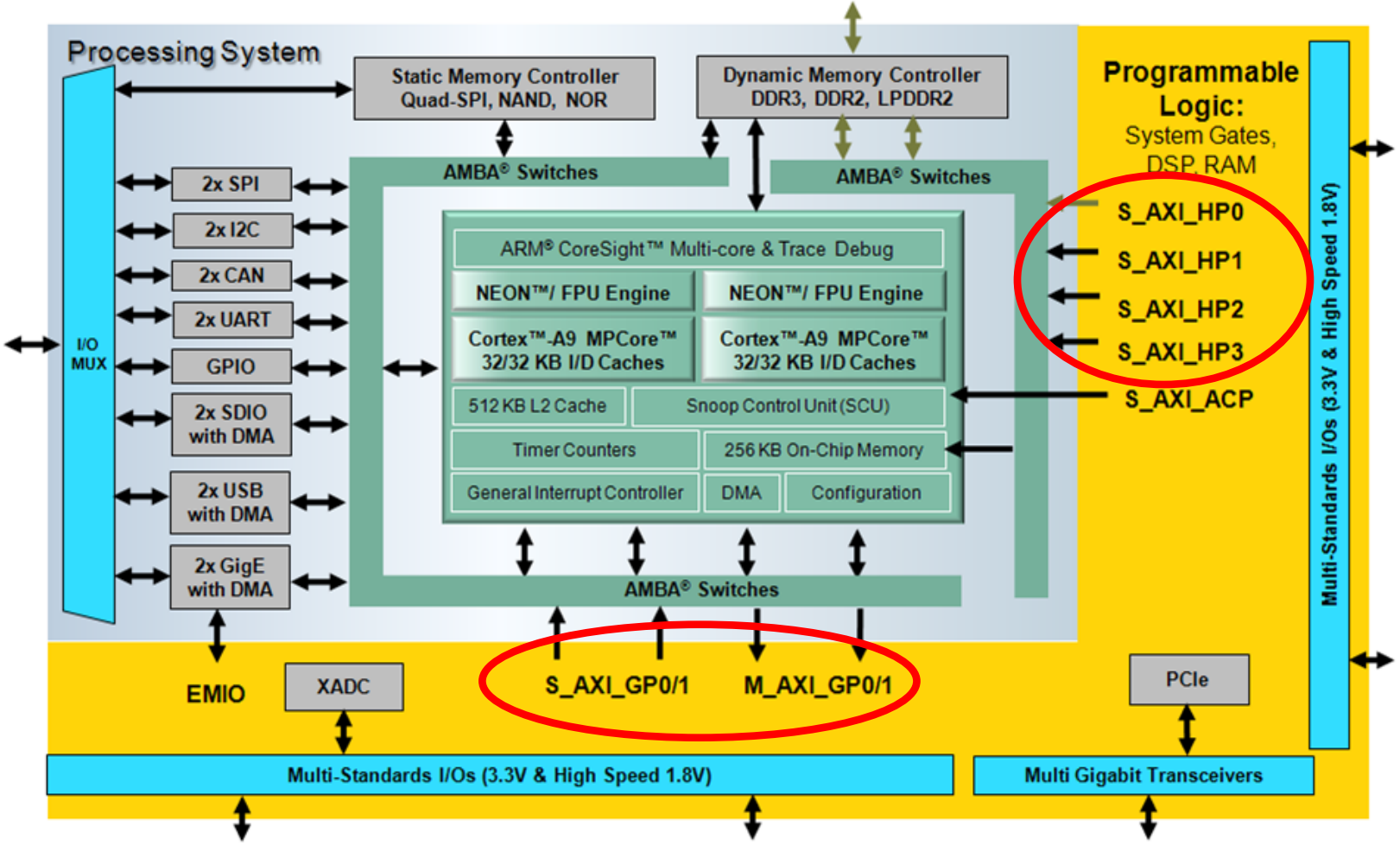
- Multiplexed Input/Output (MIO)
  - Multiplexed output of peripheral and static memories
- Extended MIO
  - Extension with PL side IOs
  - Additional interface with PL cores



PS – PL Interface

- **AXI high-performance slave ports (HP0-HP3)**
  - Configurable 32-bit or 64-bit data width
  - Access to OCM and DDR only
  - Conversion to processing system clock domain
  - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth large data transfers
- **AXI general-purpose ports (GP0-GP1)**
  - Two masters from PS to PL
  - Two slaves from PL to PS
  - 32-bit data width
  - Conversation and sync to processing system clock domain

Zynq-7000 SoC Block Diagram



PS – PL Interface

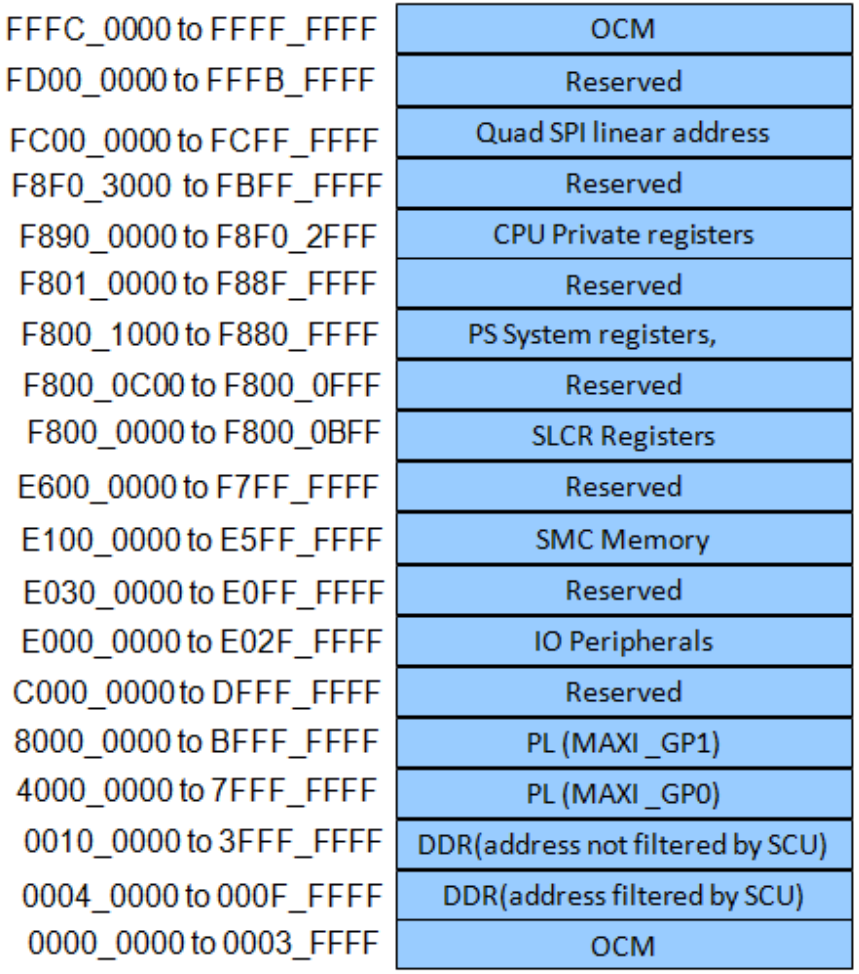
Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL
S_AXI_GP0	General Purpose (AXI_GP)	PL	PS
S_AXI_GP1		PL	PS
S_AXI_ACP	Accelerator Coherency Port (ACP), cache coherent transaction	PL	PS
S_AXI_HP0	High Performance Ports (AXI_HP) with read/write FIFOs. (Note that AXI_HP interfaces are sometimes referred to as AXI Fifo Interfaces, or AFIs).	PL	PS
S_AXI_HP1		PL	PS
S_AXI_HP2		PL	PS
S_AXI_HP3		PL	PS

PS – PL Interface

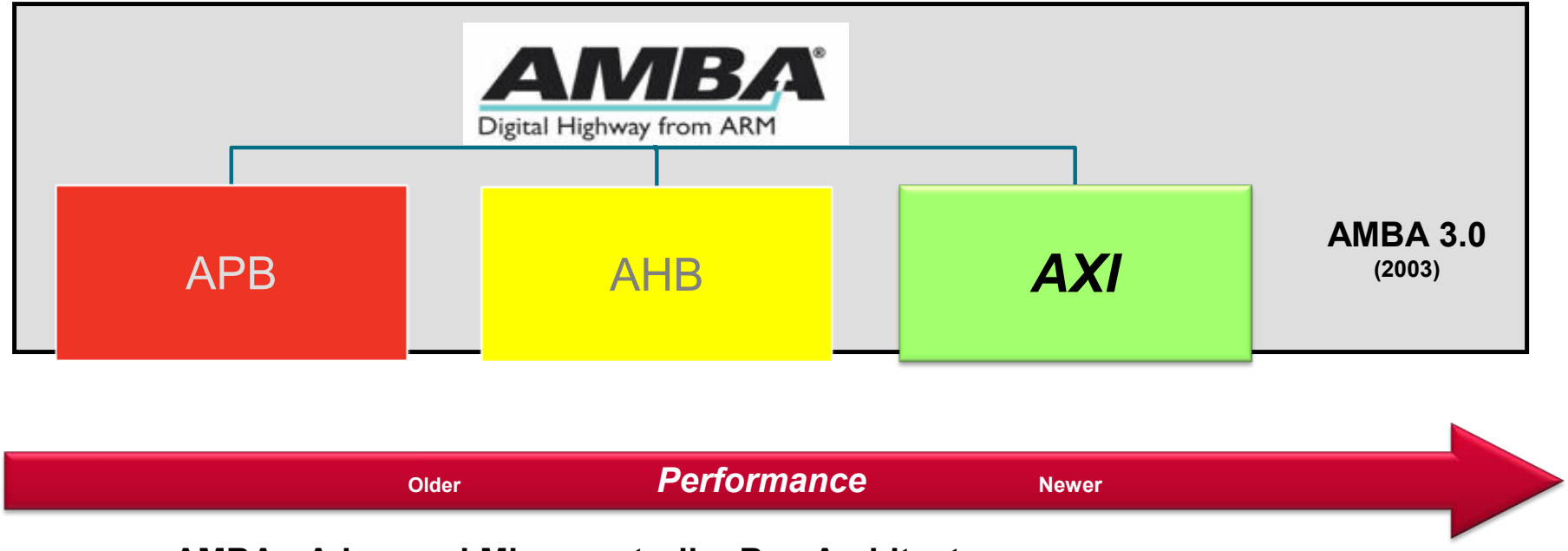
- DMA, interrupts, events signals
  - Processor event bus for signaling event information to the CPU
  - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
- Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins

Memory Map

- The Cortex-A9 processor uses 32-bit addressing
- All PS/PL peripherals are memory mapped to the A9 cores
- All PL slave peripherals are located between
  - 4000_0000 -- 7FFF_FFFF (connected to GP0)
  - 8000_0000 -- BFFF_FFFF (connected to GP1)



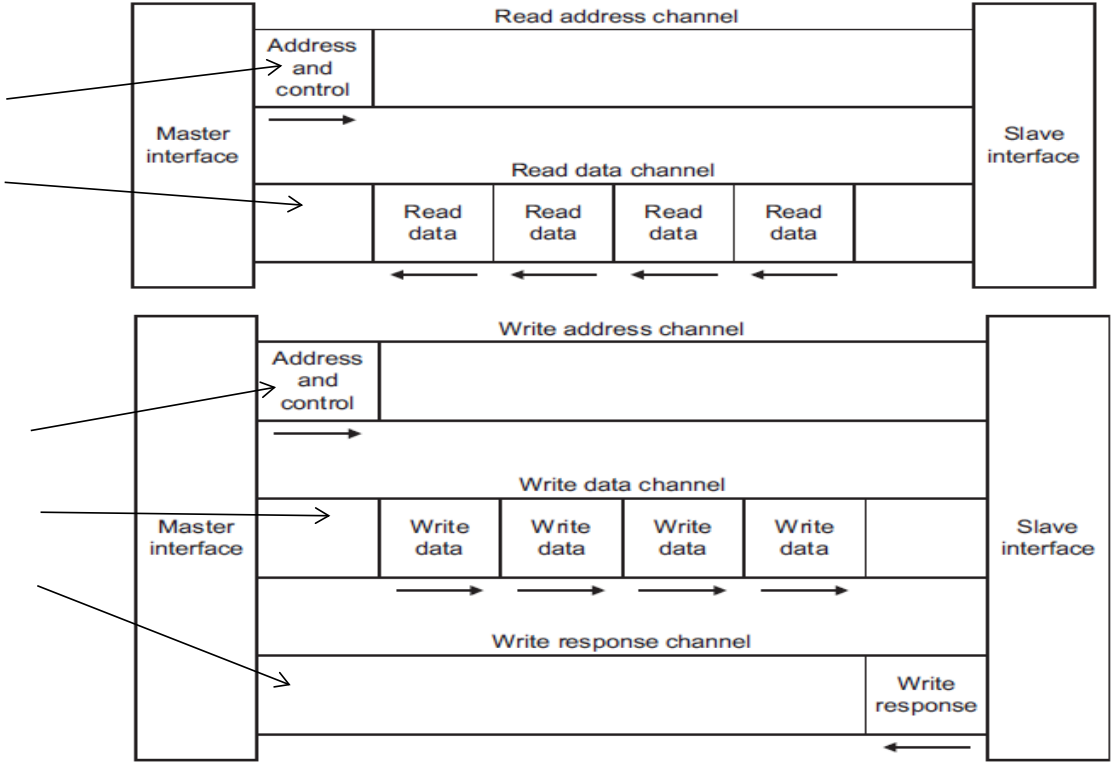
AXI Interface



AMBA: Advanced Microcontroller Bus Architecture
AXI: Advanced Extensible Interface

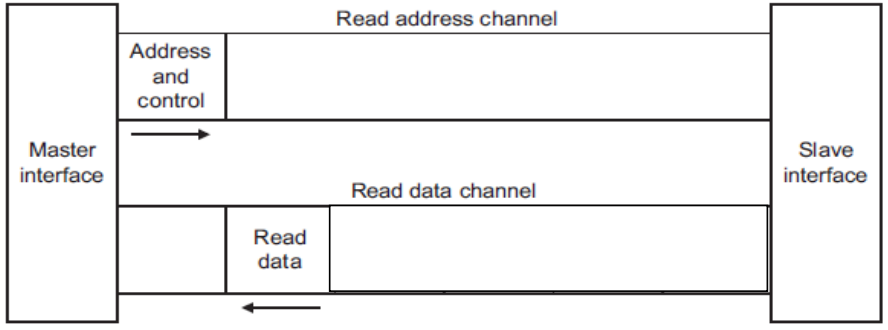
Basic AXI Protocol

1. Read Address Channel
2. Read Data Channel
3. Write Address Channel
4. Write Data Channel
5. Write Response Channel

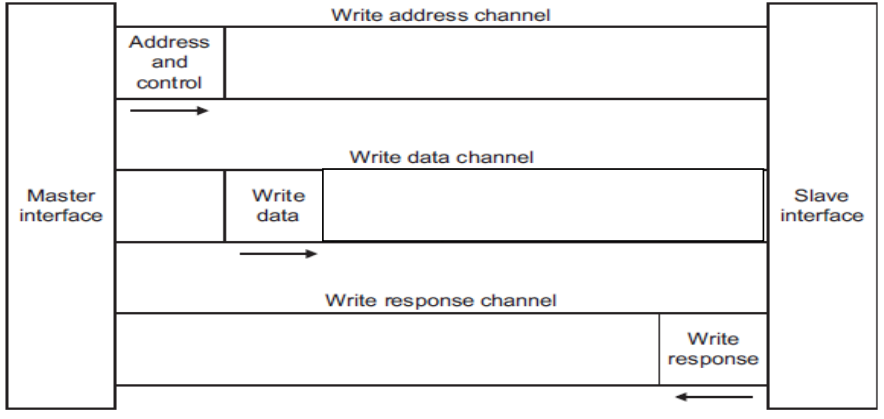


AXI4—Lite Protocol

- **No burst**
- **Data width 32 or 64 only**
  - Xilinx IP only supports 32-bits
- **Very small footprint**
- **Bridging to AXI4 handled automatically by AXI_Interconnect (if needed)**



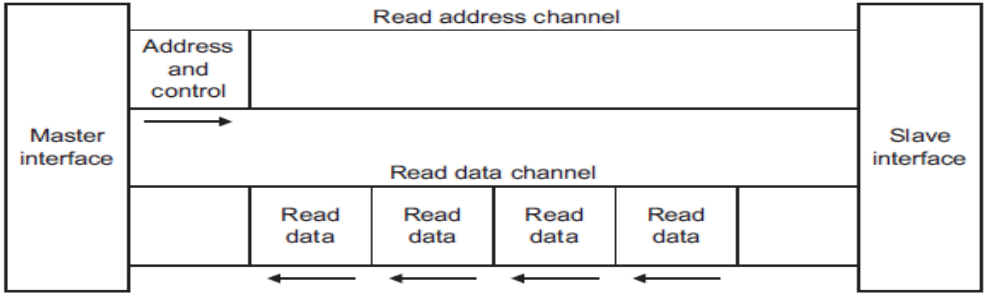
AXI4-Lite Read



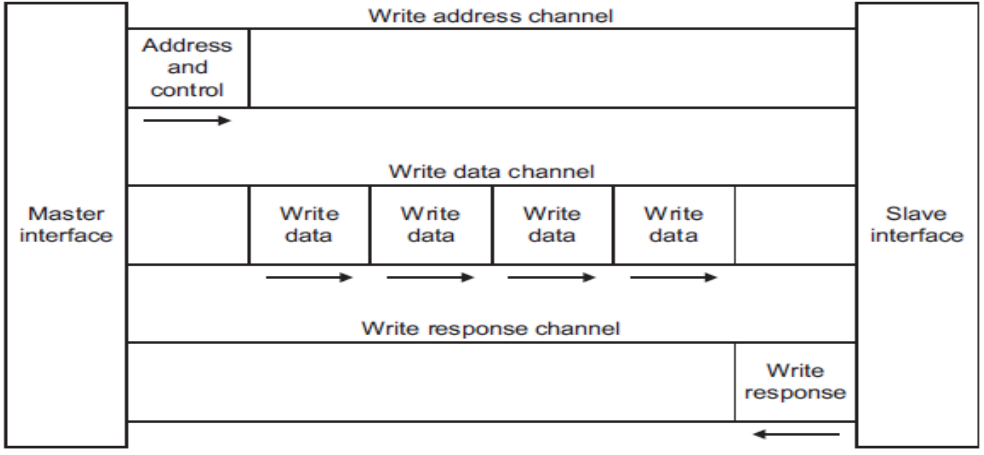
AXI4-Lite Write

AXI4 Protocol

- **Sometimes called "Full AXI" or Memory Mapped"**
  - Not ARM-sanctioned names
- **Single address multiple data**
  - Burst up to 256 data beats
- **Data Width parameterizable**
  - 1024 bits



AXI4 Read

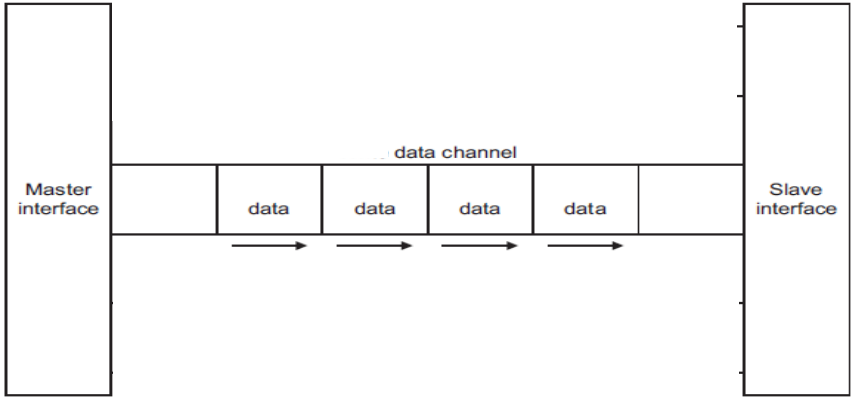


AXI4 Write

AXI4—Stream Protocol

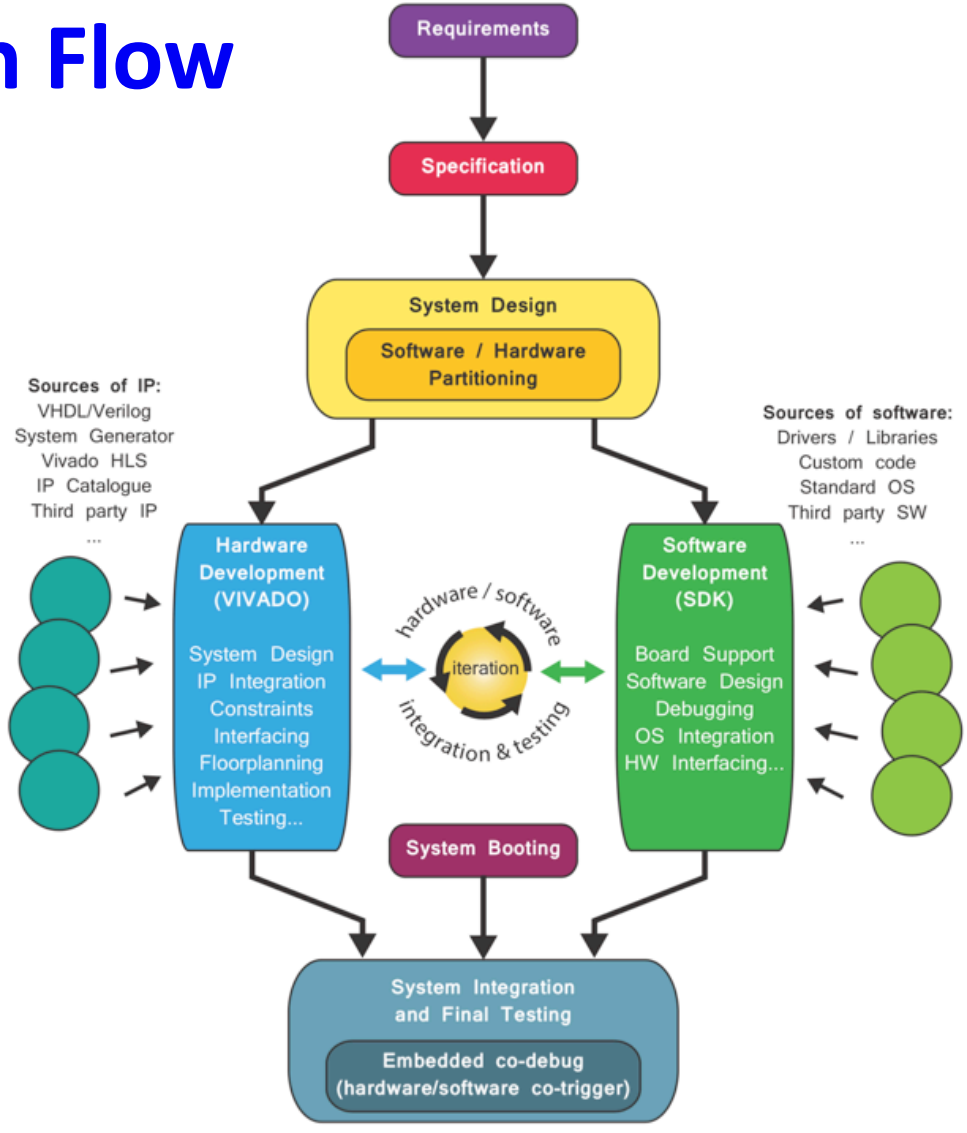
- **No address channel, no read and write, always just master to slave**
  - Effectively an AXI4 “write data” channel
- **Unlimited burst length**
  - AXI4 max 256
  - AXI4-Lite does not burst
- **Virtually same signaling as AXI Data Channels**
  - Protocol allows merging, packing, width conversion
  - Supports sparse, continuous, aligned, unaligned streams

AXI4-Stream Transfer

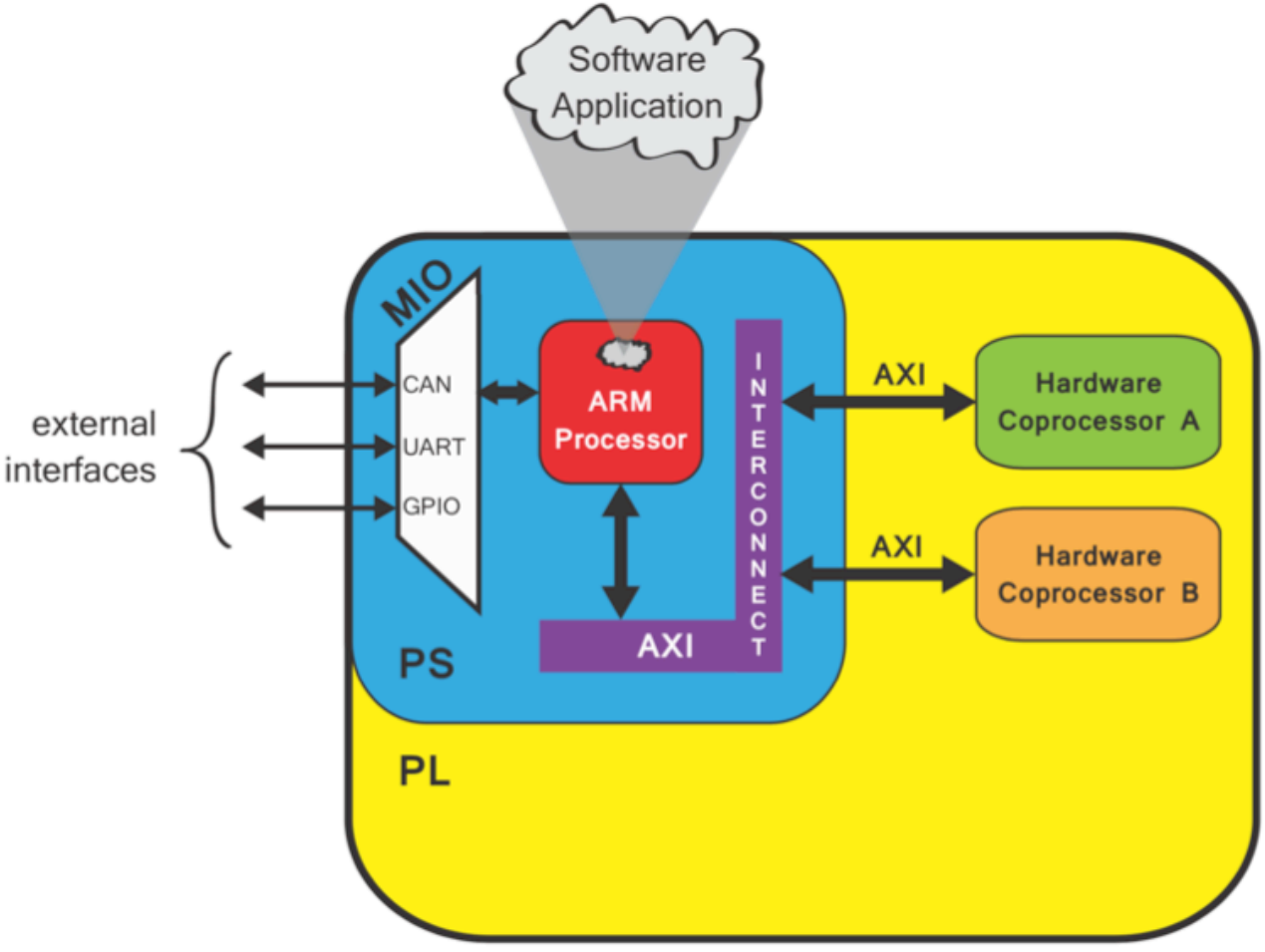


Basic Zynq Design Flow

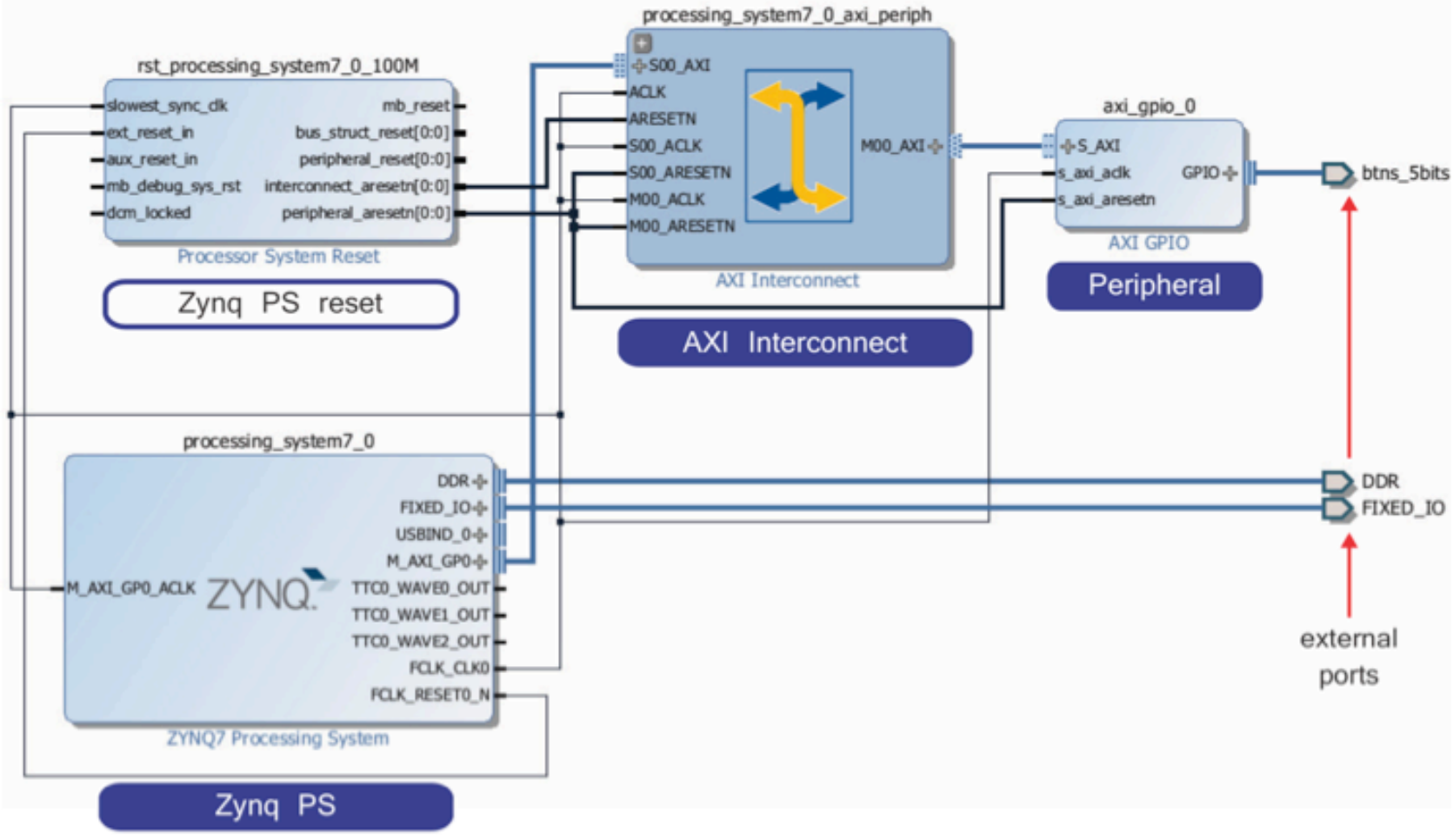
Source: The Zynq Book



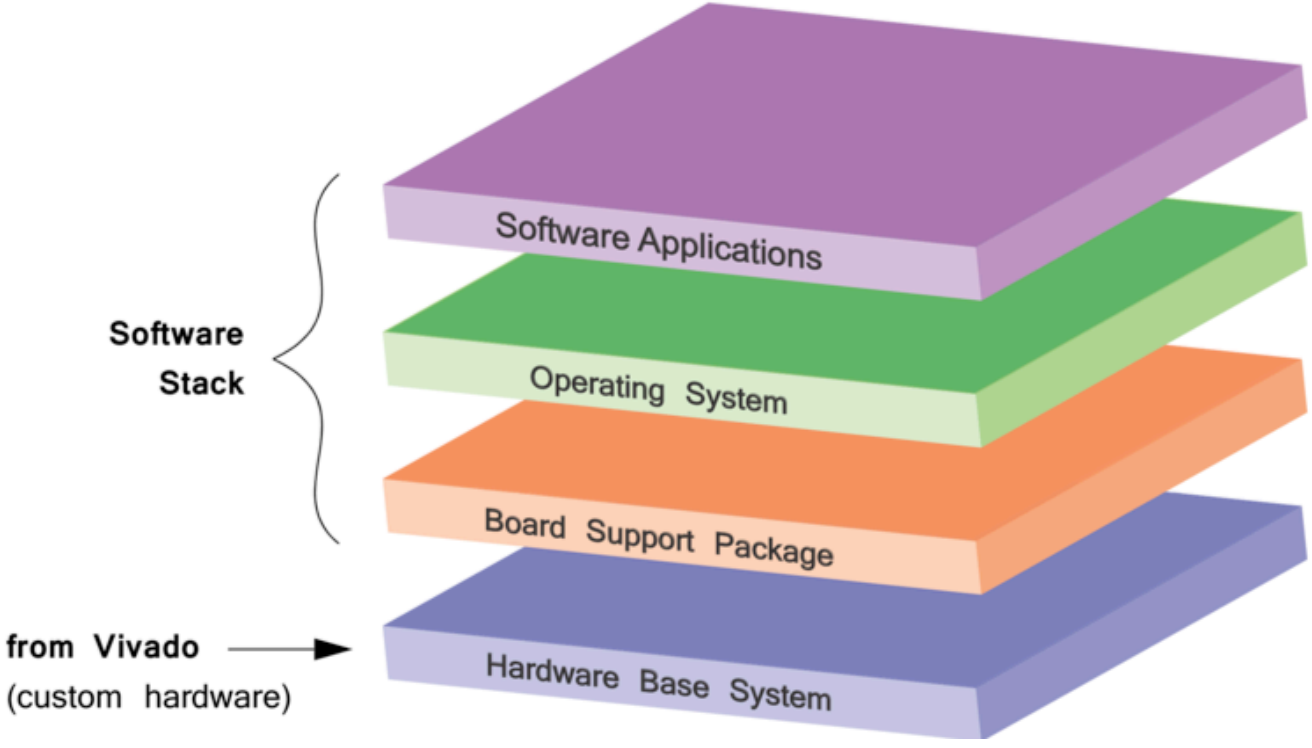
Hardware Development



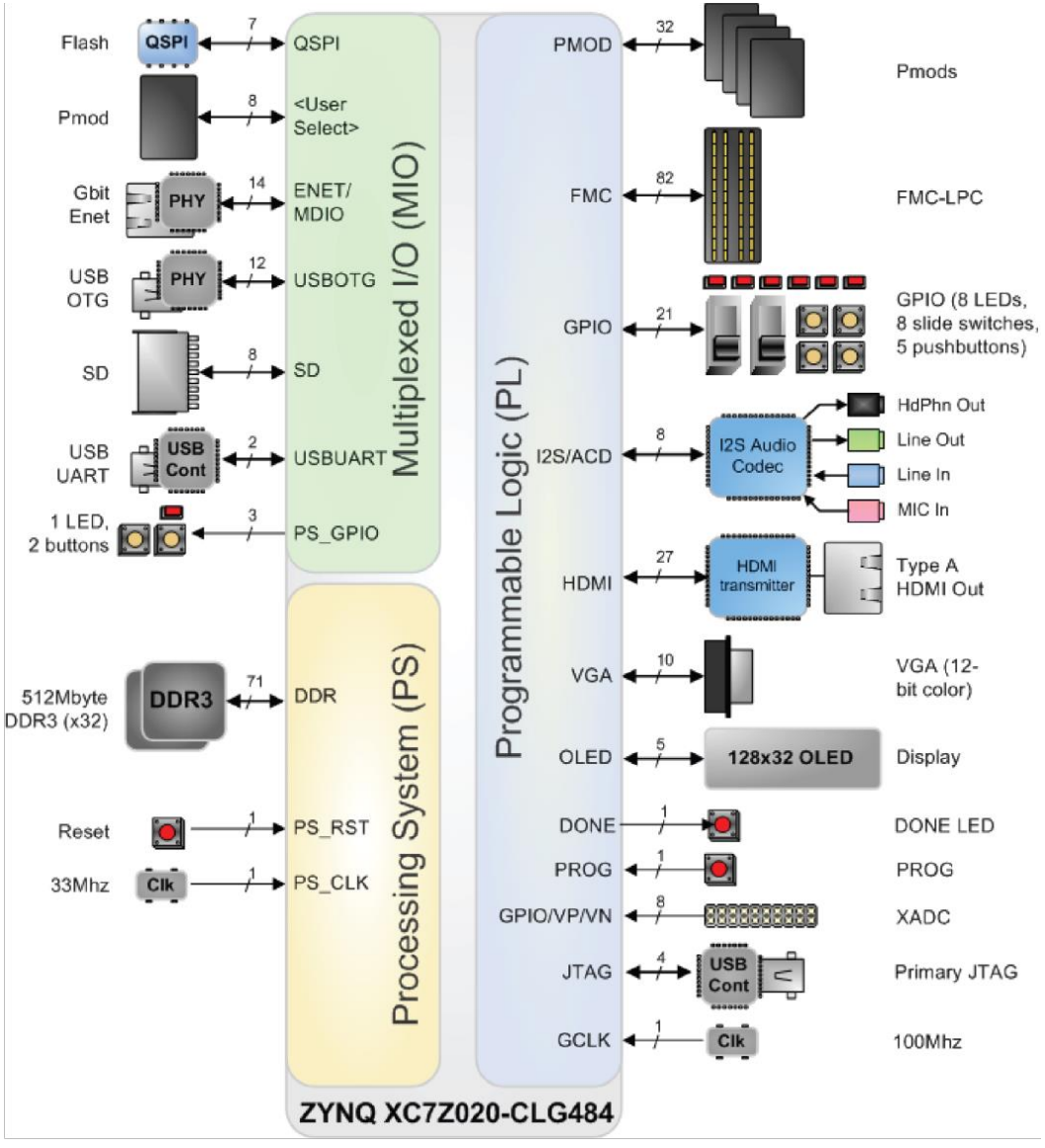
Hardware Development



Software Development



- BSP includes low-level SW routing interfacing with HW
- Refreshed by SDK when HW base is changed


Flash
QSPI
7
QSPI
Pmod
8
<User Select>
Gbit Enet
PHY
14
ENET/ MDIO
USB OTG
PHY
12
USBOTG
SD
8
SD
USB UART
USB Cont
2
USBUART
1 LED, 2 buttons
3
PS_GPIO
Multiplexed I/O (MIO)
512Mbyte DDR3 (x32)
DDR3
71
DDR
Reset
1
PS_RST
33Mhz
Clk
1
PS_CLK
Processing System (PS)
PMOD
32
Pmods
FMC
82
FMC-LPC
GPIO
21
GPIO (8 LEDs, 8 slide switches, 5 pushbuttons)
I2S/ACD
8
I2S Audio Codec
HdPhn Out
Line Out
Line In
MIC In
HDMI
27
HDMI transmitter
Type A HDMI Out
VGA
10
VGA (12-bit color)
OLED
5
128x32 OLED
Display
DONE
1
DONE LED
PROG
1
PROG
GPIO/VP/VN
8
XADC
JTAG
4
USB Cont
Primary JTAG
GCLK
1
Clk
100Mhz
Programmable Logic (PL)
ZYNQ XC7Z020-CLG484

References

- Zedboard Hardware User Guide
- The Zynq Book
  - Chapter 1, 2, 3
- The Zynq 7000 SoC Technical Reference Manual