CDA 4253/CIS 6930
FPGA System Design

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Introduction

• Traditional approaches to computation: HW & SW
• HW (ASICs – Application Specific ICs)
  – Fixed on a particular application
  – Efficient: performance, silicon area, power
  – Higher cost/per application
• SW on microprocessors
  – Programmability: used in many applications
  – Less efficient: performance, silicon area, power
  – Lower cost/per application
Introduction

• **Field Programmable Gate Arrays (FPGAs)**
  – *Spatial computing*: similar to HW
  – *Reprogrammable*: similar to SW
  – Faster than SW and more flexible than HW
  – More cost-effective for low volume applications
  – Harder to program than SW
  – Less efficient than HW: performance, silicon area, power

• But ASIC HW is going away — design cost too high
  – FPGA design is promising!
Course Descriptions

• Overview of FPGA architectures
  – Basic building blocks
  – Field programmability
• Digital design with VHDL
  – Learn to write VHDL for synthesis and simulation
  – Analyze and understand existing examples
  – Modify or use the existing examples for new designs
• Basic concepts of FPGA design flow
• Basic Ideas of high-level synthesis
  – Mapping from algorithms to VHDL.
• Other relevant topics: heterogeneous computing, partial reconfiguration, etc
Course Outcomes

• Use **VHDL** for design/simulation/synthesis
  – One of the most basic and sought-after skills
• Understanding of high-level synthesis
• Knowledge of state-of-the-art **FPGA Design tools** used in the industry
• Knowledge & experiences of a modern **FPGA platform**.
• A **design portfolio** that can be added to your resume.
Course Descriptions

• No required textbook. But, you need access to a good VHDL reference book.
• We will use the following book extensively.
  – *FPGA Prototyping by VHDL Examples* by Chu.
  – VHDL code in the book is available at [here](#).
• Additional reading materials will be distributed.
• Required background: CDA 3201/3201L
• Attendance is required.
Reference Books

Part I Basic Digital Circuits
- combinational
- sequential
- state machines

Part II EMBEDDED SOC I: VANILLA FPRO SYSTEM video

Part III EMBEDDED SOC II: BASIC I/O CORES

PART IV EMBEDDED SOC III: VIDEO CORES

available online from USF library
Reference Books

available at http://www.zynqbook.com
Course Descriptions: Evaluation

• Around 6 lab assignments: 60%
  – Each assignment includes design problems.
  – All assignments are individual unless specified otherwise.

• One final project: 40%

• Final grading scale:

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<th>Grade</th>
<th>Percentage</th>
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<tr>
<td>F</td>
<td>&lt; 60%</td>
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<td>80% – 89.99%</td>
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• Be Honest!
  – Collaborate, but do not copy each other’s work.
  – Anyone found cheating (all parties) will get FF.
Office Hour

• Instructor
  – Time: 2:30-4pm, Mon. & Wed, or by appointment.
  – Office: ENB 312
  – Email: haozheng@usf.edu
  – Office phone: 813-874-4757
Course Communication

• Canvas:
  – Announcements
  – Download assignment descriptions
  – Submit your solutions
  – Check your grades
  – Discussions where you can collaborate

• [www.cse.usf.edu/~haozheng/teach/cda4253](http://www.cse.usf.edu/~haozheng/teach/cda4253)
  – Slides
  – Other course related documents
Course Topics

• Digital Design with VHDL
  – Modeling/synthesis/simulation
• FPGA architectures
  – Commercial (Xilinx / Altera)
• Basic concepts of FPGA CAD algorithms
• Basic idea of high-level synthesis
• Heterogeneous computing
• Case studies
• Other selected topics if time permits
Zedboard – Overview
Zedboard Information

• More related information can be found at
  – Digilent’s website
  – **Digilent Zedboard resource center**
  – *zedboard.org*
Vivado Design Suite

• An environment where you create VHDL descriptions of designs.

• Offers tools for
  – simulation, synthesis, FPGA configuration

• The version for this course:

  Vivado HLx 2018.1 Webpack (free)
  – All your work will be evaluated with this tool
Vivado – Documents

• Vivado Design Suite User Guide -- Getting Started
  – Master guide
• Vivado® Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)
• Vivado Design Suite User Guide: Using the Vivado IDE (UG893)
• More information at xilinx.com Vivado HLx page

• Tutorial: Getting Started with Vivado
  – https://reference.digilentinc.com/vivado/getting_started/start