CDA 3201 Digital Logic Design

Instructor:	Dr. Hao Zheng
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Office Hour/location:	Tue. $3-4pm$, Fri. $10-11am$, or by appointment.
Calss Meeting Time/Location:	Tue., Thr., $12:30am-1:45pm$ at CHE 303.
Credit Hours:	3

Teaching Assistant:

Name	Office	Office Hours	Email
Michael Nachtigal	ENB 325	Wed. 1 - 4pm	mnachtig@mail.usf.edu
Caitrin Eaton	ENB 325	Mon. 1 - 4pm	caitrin.eaton@gmail.com
Yangwei Cai	ENB 325	Thr. 2:30 - 5:30pm	ycai@mail.usf.edu
Vladimir Grupcev	ENB 325	Tue 2 - 3pm and 4 - 6 pm	vgrupcev@mail.usf.edu

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Course Description

This is an introductory course in digital logic circuits covering number representation, digital encodings, Boolean Algebra, combinatorial logic design, sequential logic design, and programmable logic devices. The course will introduce the basic building blocks implementing various digital operations, and techniques mapping from specification to logic networks. Issues that need to be considered for digital designs will also be discussed. This course should prepare students for more advanced courses in computer system design, design automation, and other courses in computer science.

Textbook Langholz, Kandel, & *Mott, Foundations of Digital Logic Design*, World Scientific Publishing, ISBN 981-02-3110-5.

Grading and Attendance Students will not be graded on attendance or participation, but both are strongly recommended in order to successfully complete the course. Incomplete grades will be given only if specific documentation of necessity is presented. The grade will be based on three in-class exams, and graded homeworks. The grades will be weighted as follows:

Homeworks/Quizzes:	15%
Midterm Exam 1:	25%
Midterm Exam 2:	30%
Final:	30%

The grading scale is as follows:

A:	> 90
B:	80 - 89.9
C:	70 - 79.9
D:	60 - 69.9
F:	< 60

Examinations There are three examinations given for this course. Make up exams will be given for documented emergencies only with advance notices.

Homeworks Several homework assignments will be given over the course of the semester. These are exercises which will hone your problem solving skills while giving you a preview of the test questions as well. The homework assignments will be designated as *required* or *optional*. The *required* homeworks shall be graded and will account to your final course grade. You are encouraged to solve the *optional* homework problems in order to get more practice which will make you more confident in the course material.

Note: make sure the specific requirements for each homework assignment are read carefully; otherwise significant losses of credits may be incurred if any of the requirements is not met for submissions.

Last Day to Drop with 'W' October 27.

Final Exam Week December $4 - 10$

Academic Integrity and Dishonesty Students are expected to be honest and not cheat on their assignments/examinations/project. Collaboration and discussion with fellow students are highly encouraged, but copying each other's work is forbidden. Every student should read the University's policies on student conduct, academic dishonesty, etc. Please see the University's Undergraduate Catalog regarding these policies at `http://www.ugs.usf.edu/catalogs/0809/adadap.htm`. Students caught cheating in any form will receive an **FF** grade for the course.

Tentative Schedule

Date	Topic
8/24	Chapter 1 Introduction
8/26	Chapter 1 Introduction
8/31	Chapter 2 Number Representations
9/2	Chapter 2 Number Representations
9/7	Chapter 3 Boolean Algebra
9/9	Chapter 3 Boolean Algebra
9/14	Chapter 3 Boolean Algebra
9/16	Review of Chapter 1, 2, and 3, Chapter 4 Combination Logic Circuits
9/21	Midterm 1
9/23	Chapter 4 Combination Logic Circuits
9/28	Chapter 4 Combination Logic Circuits
9/30	Chapter 4 Combination Logic Circuits
10/5	Chapter 5 Combination Circuit Implementation
10/7	Chapter 5 Combination Circuit Implementation
10/12	Chapter 5 Combination Circuit Implementation
10/14	Review of Chapter 4 and 5, Chapter 6 Async. Seq. Circuits
10/19	Midterm 2
10/21	Chapter 6 Async. Seq. Circuits
10/26	Chapter 6 Async. Seq. Circuits
10/28	Chapter 6 Async. Seq. Circuits
11/2	Chapter 6 Async. Seq. Circuits
11/4	Chapter 7 Sync. Seq. Circuits
11/9	Chapter 7 Sync. Seq. Circuits
11/11	Veteran's Day, no class
11/16	Chapter 7 Sync. Seq. Circuits
11/18	Chapter 7 Sync. Seq. Circuits
11/23	Chapter 7 Sync. Seq. Circuits
11/25	Thanksgiving Holiday, no class
11/30	Chapter 7 Sync. Seq. Circuits
12/2	Review of Chapter 6 and 7.
TBD	Final Exam